IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ANALOG DEVICES, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. _____
	)	
XILINX, INC.,	)	**JURY TRIAL DEMANDED**
	)	
Defendant.	)	

COMPLAINT

Analog Devices, Inc. ("ADI"), by and through the undersigned counsel, brings this action for patent infringement against defendant Xilinx, Inc. ("Xilinx").

INTRODUCTION

1. ADI is the global market leader and innovator in the design and manufacture of high performance analog, mixed signal, and power integrated circuit products. ADI gained this leadership through hard work, a commitment to excellence, and substantial economic investments.

2. This case arises out of Xilinx's recent attempts to incorporate ADI's patent-protected inventions into Xilinx's products.

PARTIES

3. ADI is a Massachusetts corporation with its corporate headquarters located at One Technology Way, Norwood, Massachusetts 02062.

4. ADI's products are embedded inside many different types of electronics devices, and used around the world in diverse industries including, for example, aerospace and defense, computer networking, cellular and wireless infrastructure, automobiles, industrial process and control systems, medical imaging equipment, and consumer portable electronics. As the world's

leading provider of high-performance data converters, ADI offers both the largest analog-to-digital converter (ADC) portfolio and largest digital-to-analog converter (DAC) portfolio in the industry. Confirming this technical leadership, ADI has been named a Top 100 Global Innovator seven times in the last eight years, and was recently awarded the IEEE Corporate Innovation Award for sustained innovation and leadership in the development of high-performance data converter technology and products. ADI's award-winning products have been consistently recognized as pushing the boundaries in critical areas including sample rate, dynamic range, power efficiency, and integration.

5. Founded in 1965 by Ray Stata and Matthew Lorber, both graduates of the Massachusetts Institute of Technology, ADI has fostered a culture of innovation. Mr. Stata's visionary leadership transformed ADI from its beginnings as a small Cambridge-based company into a global technology company offering one of the most comprehensive and technologically sophisticated lines of integrated circuits in the world. In 1969, ADI made its first foray into the semiconductor business and rose to the challenge of rivaling larger companies that already had a head start in the newly developing space. ADI has since established itself as a leading supplier of high-performance analog-to-digital converters that emphasize speed and precision.

6. On information and belief, defendant Xilinx, Inc. is a Delaware corporation, with a principal business address of 2100 Logic Drive, San Jose, California 95124.

JURISDICTION AND VENUE

7. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338.

8. This Court has personal jurisdiction over Xilinx. Xilinx is a Delaware corporation and has continuous and systematic business contacts with the State of Delaware. Xilinx, directly and through subsidiaries or intermediaries (including distributors, retailers, and

others), has purposefully and voluntarily placed its infringing products and services into this District and into the stream of commerce with the intention and expectation that they will be purchased and used by consumers in this District. Xilinx has offered and sold and continues to offer and sell these infringing products and services in this District.

9. Venue is proper in this District pursuant to 28 U.S.C. §1400(b) because Xilinx is a Delaware corporation.

FACTUAL ALLEGATIONS

ADI's Patented Technologies

10. ADI has become the world's leading provider of data conversion technology through hard work, a commitment to excellence, and substantial economic investments. In the last five years alone, the company has invested more than $5 billion in research and development, much of it focused on ADCs, DACs, and related circuit and system design challenges. This continuing investment in innovation has produced one of the industry's top patent portfolios, including over 3,200 patents in the United States and many more across the globe.

11. This complaint focuses on eight important ADI patents relating to ADCs.

12. ADI is the assignee and owner of United States Patent No. 7,719,452 titled "Pipelined Converter Systems With Enhanced Linearity" (the "'452 Patent"). The '452 Patent was duly and legally issued on May 18, 2010. The patent relates generally to a circuit and technique for enhancing linearity in analog-to-digital converters by injecting dither to sampled signals. A copy of the '452 Patent is attached as Exhibit A.

13. ADI is the assignee and owner of United States Patent No. 7,663,518, titled "Dither Technique For Improving Dynamic Non-linearity In An Analog To Digital Converter, And An Analog To Digital Converter Having Improved Dynamic Non-linearity" (the "'518

Patent"). The '518 patent was duly and legally issued on Feb. 16, 2010. The patent relates generally to a circuit and technique for applying a dither to improve linearity. A copy of the '518 Patent is attached as Exhibit B.

14. ADI is the assignee and owner of United States Patent No. 6,900,750 titled "Signal Conditioning System With Adjustable Gain And Offset Mismatches" (the "'750 Patent"). The '750 Patent was duly and legally issued on May 31, 2005. The patent relates generally to a circuit and technique for calibrating an offset mismatch in analog-to-digital converters using chopping techniques. A copy of the '750 Patent is attached as Exhibit C.

15. ADI is the assignee and owner of United States Patent No. 10,250,250, titled "Bootstrapped Switching Circuit," (the "'250 Patent"). The '250 Patent was duly and legally issued on April 2, 2019. The patent relates generally to a circuit and technique for quickly activating a switch, such as a front-end sampling switch, by generating a boosted voltage using a positive feedback loop. A copy of the '250 Patent is attached as Exhibit D.

16. ADI is the assignee and owner of United States Patent No. 7,274,321, titled "Analog to Digital Converter" (the "'321 Patent"). The '321 Patent was duly and legally issued on September 25, 2007. The patent relates generally to analog-to-digital converters having a pipelined converter architecture. A copy of the '321 Patent is attached as Exhibit E.

17. ADI is the assignee and owner of United States Patent No. 7,012,463, titled "Switched Capacitor Circuit with Reduced Common-Mode Variations" (the "'463 Patent"). The '463 Patent was duly and legally issued on March 14, 2006. The patent relates generally to switched capacitor circuits that provide a feedback signal to reduce common-mode variations in an output of a circuit. A copy of the '463 Patent is attached as Exhibit F.

18. ADI is the assignee and owner of United States Patent No. 8,487,659, titled "Comparator with Adaptive Timing" (the "'659 Patent"). The '659 Patent was duly and legally issued on July 16, 2013. The patent relates generally to timing circuits that compensate for the effects of variations in process, voltages, and temperature. A copy of the '659 Patent is attached as Exhibit G.

19. ADI is the assignee and owner of United States Patent No. 7,286,075, titled "Analog to Digital Converter with Dither" (the "'075 Patent"). The '075 Patent was duly and legally issued on October 23, 2007. The patent relates generally to a circuit and technique for enhancing linearity in analog-to-digital converters by injecting dither to sampled signals. A copy of the '075 Patent is attached as Exhibit H.

Xilinx's Incorporation of Analog's Patented Technologies into Xilinx's RFSoC Products

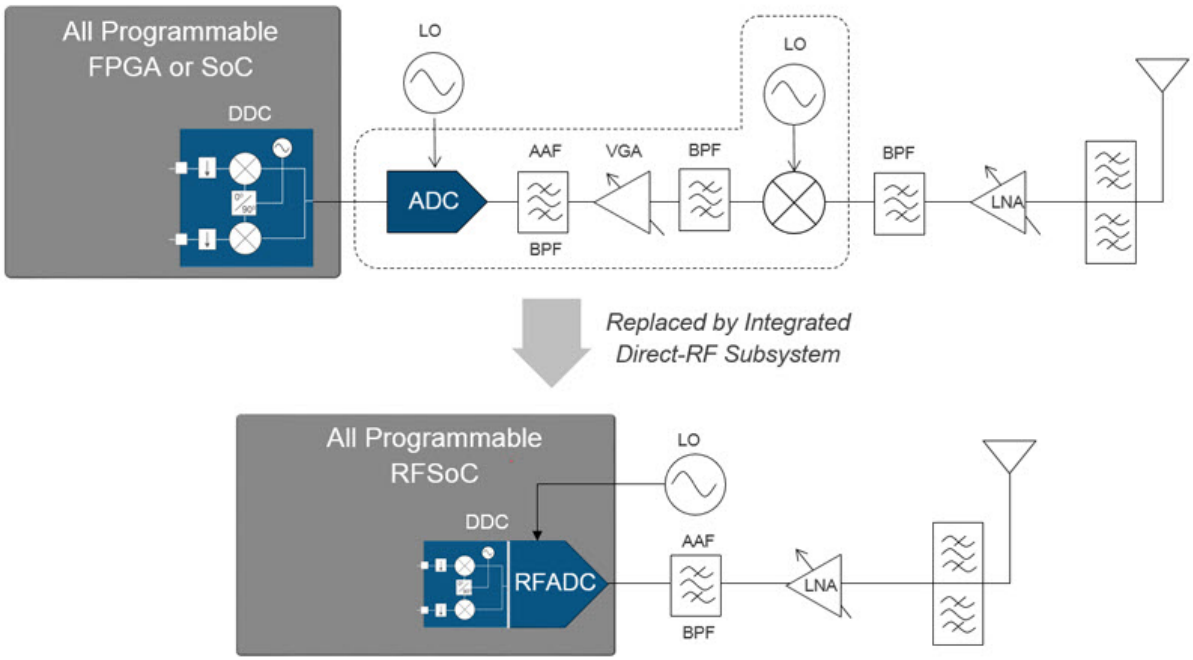
20. Xilinx has been a significant beneficiary of ADI's substantial and continuing investments in analog-to-digital conversion technology. ADI has worked closely with Xilinx for many years to develop proven solutions tailored to Xilinx's field-programmable gate array (FPGA) products, including Xilinx's Kintex 7 and Kintex UltraScale products, its Virtex 7 and Virtex UltraScale products, its Zynq 7 products, and its initial Zynq UltraScale products. *See, e.g.*, https://www.analog.com/en/design-center/reference-designs/hardware-reference-design/fpga-compatible-reference-designs/xilinx-fpga.html#z7.

21. Over the course of the parties' collaboration, ADI has shared with Xilinx, under a non-disclosure agreement, extensive and detailed technical information concerning its many innovations in ADC technology.

22. Xilinx has not only benefitted from its partnership with ADI but also has extensively promoted this partnership on Xilinx's own website. *See, e.g.,*

https://www.xilinx.com/alliance/memberlocator/1-8dv3-84.html; https://www.xilinx.com/video/fpga/analog-devices-demo-5gsps-data-acquisition.html. For example, Xilinx's website touts ADI as a partner that has "provide[d] a rich set of JESD204B references designs and high-speed FMC cards to jump start development." *See* https://www.xilinx.com/products/technology/high-speed-serial/jesd2014-reference-designs.html (listing, among others, ADI and its "4-chan, 14-bit, 250 MSPS" analog-to-digital converter).

23. At the same time that Xilinx purportedly was working with ADI as an alleged partner to combine ADI's proprietary ADC technology with Xilinx's programmable system-on-a-chip ("SoC") products, however, Xilinx was also separately working to incorporate ADI's patented technology directly into its new "Integrated Direct-RF Subsystem":



See https://www.xilinx.com/products/technology/rfsampling.html#overview. Contrary to its purported partnership with ADI, Xilinx boasts that its RFSoC product "[e]liminates discrete

converters" and "[r]emoves power-hungry FPGA-to-Analog interfaces like JESD204." *See, e.g.*, https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html.

24. Xilinx's newest Zynq UltraScale products – including at least the Zynq UltraScale + RFSoC with RF Data Converters and Zynq UltraScale + RFSoC with RF Data Converters and SD-FED Cores (collectively, the "Accused RFSoC Products") – have extensively incorporated ADI's proprietary and patented technologies.

25. Xilinx promotes the Accused RFSoC Products on its website as aimed at "High End" applications and specifically highlights the integrated "RF Data Converter" as a key feature. *See, e.g.*, https://www.xilinx.com/products/silicon-devices/soc.html.

26. Xilinx's own product literature confirms that its Accused RFSoC products now incorporate "Direct RF sampling" technology – like ADI's technology:

ABSTRACT

To achieve the performance required of the latest generation of wireless access, DOCSIS, and a range of Aerospace and Defense applications, direct RF-sampling technology holds the promise of increased adaptability and higher performance. Direct RF-sampling enables a new level adaptability by moving much of the RF signal processing into the digital domain, thereby eliminating much of the analog signal processing[Ref 1][Ref 2].

However, there is immense market pressure to reduce the power and footprint of these systems. The solution is to integrate RF-sampling data converters with VLSI devices using advanced CMOS technology.

Xilinx has long provided a highly flexible digital signal processing solution for a range of radio applications[Ref 3][Ref 4]. Integrating direct RF-sampling data converters enables a highly adaptable platform for radio development that also addresses many of the challenges associated with current discrete direct RF-sampling solutions.

References

1. Umesh Jayamohan, Technical Article, *Analog Devices*: "Not Your Grandfather's ADC: RF Sampling ADCs Offer Advantages in Systems Design".

See Xilinx White Paper, *An Adaptable Direct RF-Sampling Solution*, February 20, 2019 (available at https://www.xilinx.com/support/documentation/white_papers/wp489-rfsampling-solutions.pdf). As Xilinx recognizes in this paper, "Direct RF-sampling" – such as that accomplished in ADI's RF Sampling ADCs, cited as "Reference 1" to the paper – "enables a new level adaptability by moving much of the RF signal processing into the digital domain." Xilinx's stated solution within its RFSoC products is to "integrate" these "RF-sampling data converters" with Xilinx's own very large-scale integration ("VLSI") devices.

27. Xilinx posts information regarding how its Accused RFSoC Products operate on its website in various places, including but not limited to: https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html#documentation. Xilinx's RFSoC products are further described in:

- "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017 ("Vaz White Paper") (available at: https://www.xilinx.com/support/documentation/product-briefs/rfsoc-ieee-paper.pdf);
- "Zynq UltraScale+ RFSoC Data Sheet: Overview" ("RFSoC Data Sheet") (available at: https://www.xilinx.com/support/documentation/data_sheets/ds889-zynq-usp-rfsoc-overview.pdf);
- "High-speed ADCs for Wireless Base-Stations," Verbruggen et al., AACD 2019 ("Verbruggen White Paper") (attached as Exhibit I).
- "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at 2017 IEEE International Solid-State Circuits Conference ("Xilinx ISSCC Presentation");
- "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits Digest of Technical Papers, ("Vaz VLSI Paper") (attached as Exhibit J);
- U.S. Patent No. 10,033,395 to Vaz et al. (the "'395 Patent") (attached as Exhibit K);

28. Xilinx's reliance on ADI's patented inventions is pervasive throughout Xilinx's ADC design for its Accused RFSoC Products, including its most important architectural

elements. For example, at the front-end of the products, Xilinx's ADC infringes ADI's patented inventions relating to a fast front-end sampling switch, which is critically important to the converter's overall speed. Xilinx's ADC also infringes ADI's patented inventions relating to pipelined converter stages that ensure high speed and high resolution conversion. Xilinx's ADC infringes ADI's patented inventions relating to dithering and other techniques to improve the accuracy and linearity of the converter as a whole.

COUNT I
(Infringement of U.S. Patent No. 7,719,452)

29. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

30. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the '452 Patent, including at least claim 1, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

31. The Accused RFSoC Products include an analog-to-digital converter system to convert an analog input signal to a digital code. For example:

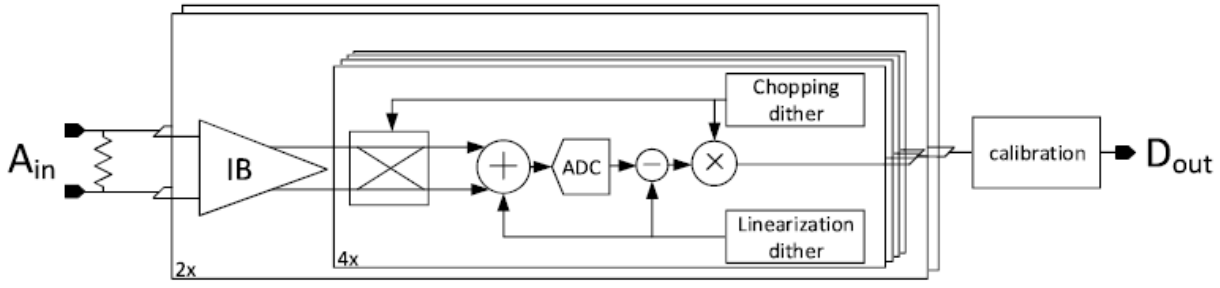


Fig.4. Simplified ADC architecture.

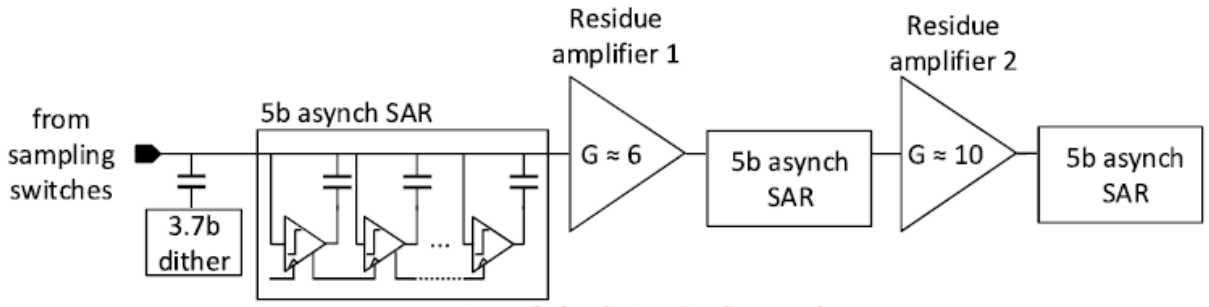


Fig. 7. Simplified ADC channel.

See, e.g., Verbruggen White Paper, Figs. 4 & 7.

32. The Accused RFSoC Products' analog-to-digital converter system has a sampler to provide samples of said analog input signal. For example, the Accused RFSoC Products' analog-to-digital converter system has a "sampling network" that provides samples of the analog input signal:

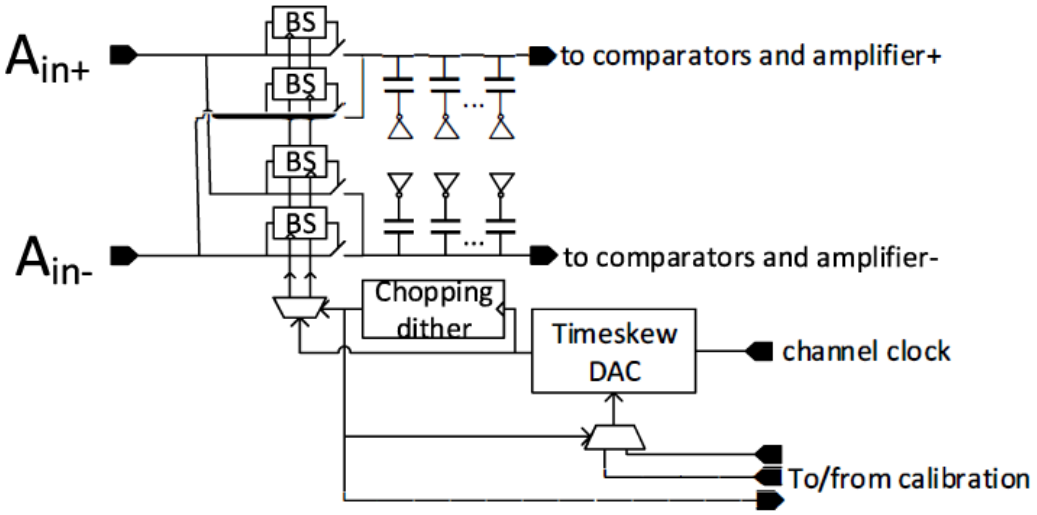


Fig. 6. Sampling network and clocking

See, e.g., Verbruggen White Paper, Fig. 6.

33. The Accused RFSoC Products' analog-to-digital converter system has signal converters arranged and configured to successively process said samples. For example, the RFSoC analog-to-digital converter system includes a 3-stage pipelined successive approximation register (SAR) architecture, where successive stages are separated by residue amplifiers. A first

stage processes an analog input signal. A second stage processes a residue signal generated by the first stage. A third stage processes a residue signal generated by the second stage. Verbruggen White Paper, Fig. 7.

34. The Accused RFSoC Products' analog-to-digital converter system has at least one digital-to-analog converter configured to respond to a random digital code and inject analog dither signals into at least a selected one of said sampler and said signal converters which process said samples and said analog dither signals into a plurality of digital codes. For example, the Accused RFSoC Products' analog-to-digital converter system has digital-to-analog converters that receive a 3.7-bit pseudo-random bit sequence and inject analog dither signals at an input of an analog-to-digital converter:

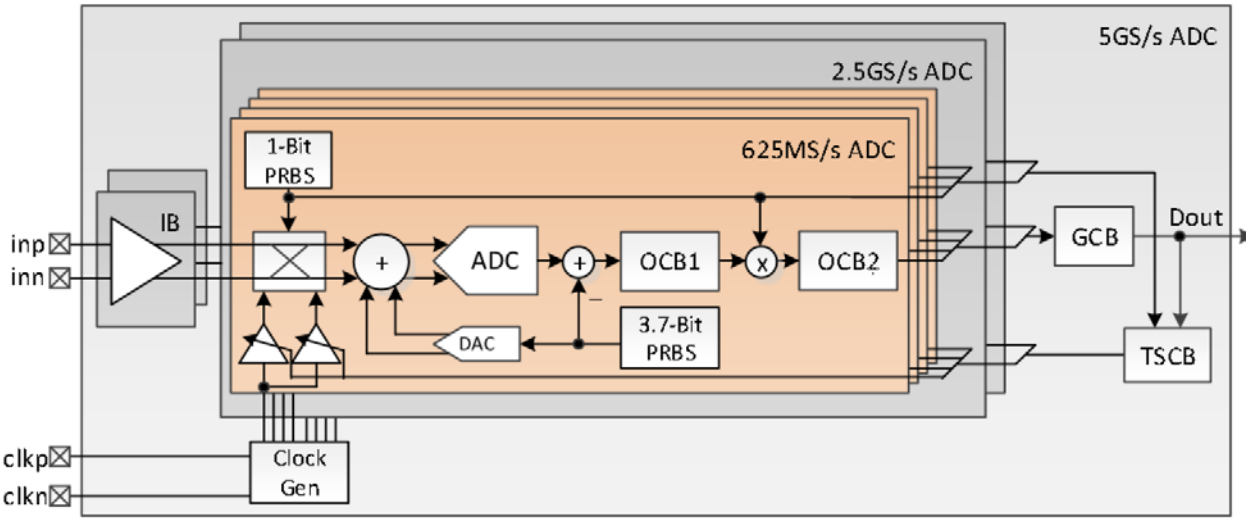


Fig. 1 ADC architecture.

See, e.g., Vaz VLSI Paper, 99.

35. The Accused RFSoC Products' analog-to-digital converter system has an aligner/corrector coupled to said signal converters to process said plurality of digital codes into a combined digital code that includes a first portion that corresponds to said samples and a second portion that corresponds to said analog dither signals. For example, the Accused RFSoC

Products include a combiner (for example, 222) that generates a digital output signal (for example, 220).

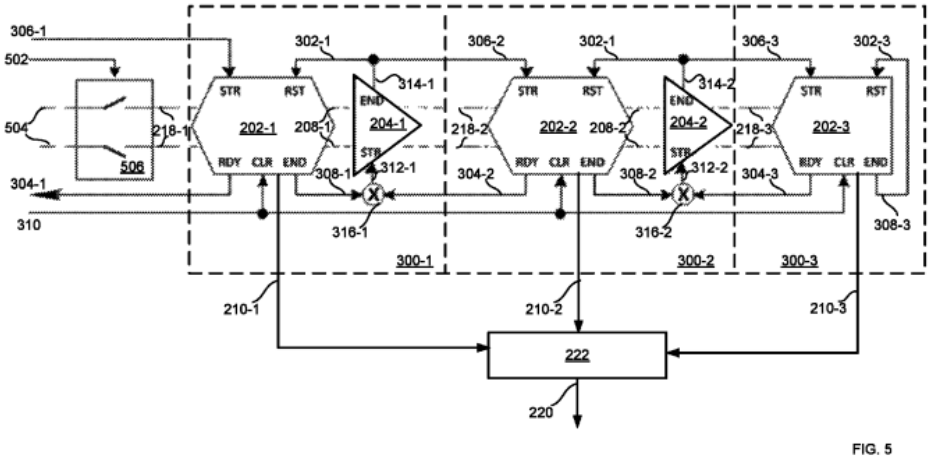


FIG. 5

See, e.g., '395 Patent, Fig. 5; *see also* Vaz VLSI Paper, Fig. 1.

36. The Accused RFSoC Products' analog-to-digital converter system has a decoder having a transfer function configured to convert said random digital code to said second portion for differencing with said combined digital code to thereby provide said system digital code. For example, the decoder in the Accused RFSoC Products' analog-to-digital converter system subtracts a digital dither signal code from the output signal of the analog-to-digital converter to provide a digitized version of the sampled signals:

Additionally, 3.7-bit PRBS dithering is injected after sampling and removed in the digital domain to further clean-up the frequency spectrum in the presence of low signal power.

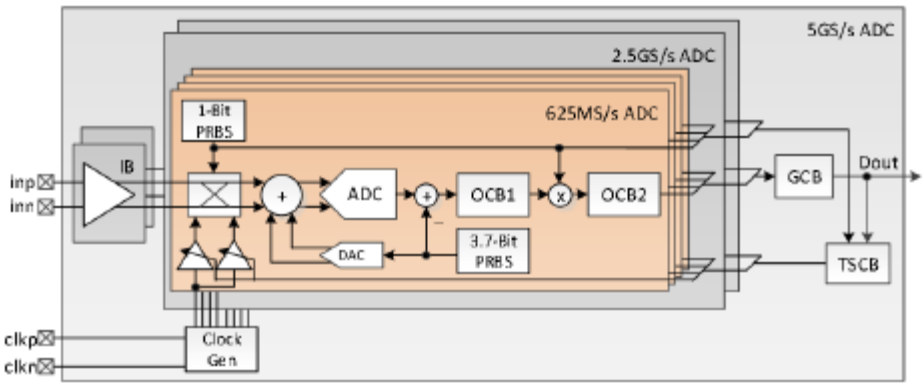


Fig. 1 ADC architecture.

See, e.g., Vaz VLSI Paper, 99.

37. In the Accused RFSoC Products' analog-to-digital converter system, said samples are thus processed along different signal-processing paths of said signal converters to thereby enhance linearity of said system. For example, a linearization dither is injected after sampling and prior to the conversion processing that is performed in the Accused RFSoC Products' analog-to-digital converters to improve linearity of the analog-to-digital converter. *See, e.g.,* Verbruggen White Paper, Fig. 4.

38. Xilinx has actively and knowingly induced, and is actively and knowingly inducing, infringement of the '452 Patent, at least by its customers' use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the '452 patent and its infringement of the '452 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx's inducement of infringement of the '452 Patent has been done with specific intent to infringe that patent.

39. Xilinx's infringement of the '452 Patent has been willful and its ongoing infringement of the '452 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI's notice, knowing that such products would infringe the '452 Patent.

40. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx's infringement of the '452 Patent.

COUNT II
(Infringement of U.S. Patent No. 7,663,518)

41. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

42. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the '518 Patent, including at least claim 1, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

43. The Accused RFSoC Products include an analog-to-digital converter that has a conversion engine comprising a switched capacitor array having redundancy. For example, the Accused RFSoC Products' analog-to-digital converters include an asynchronous pipelined-SAR analog-to-digital converter:

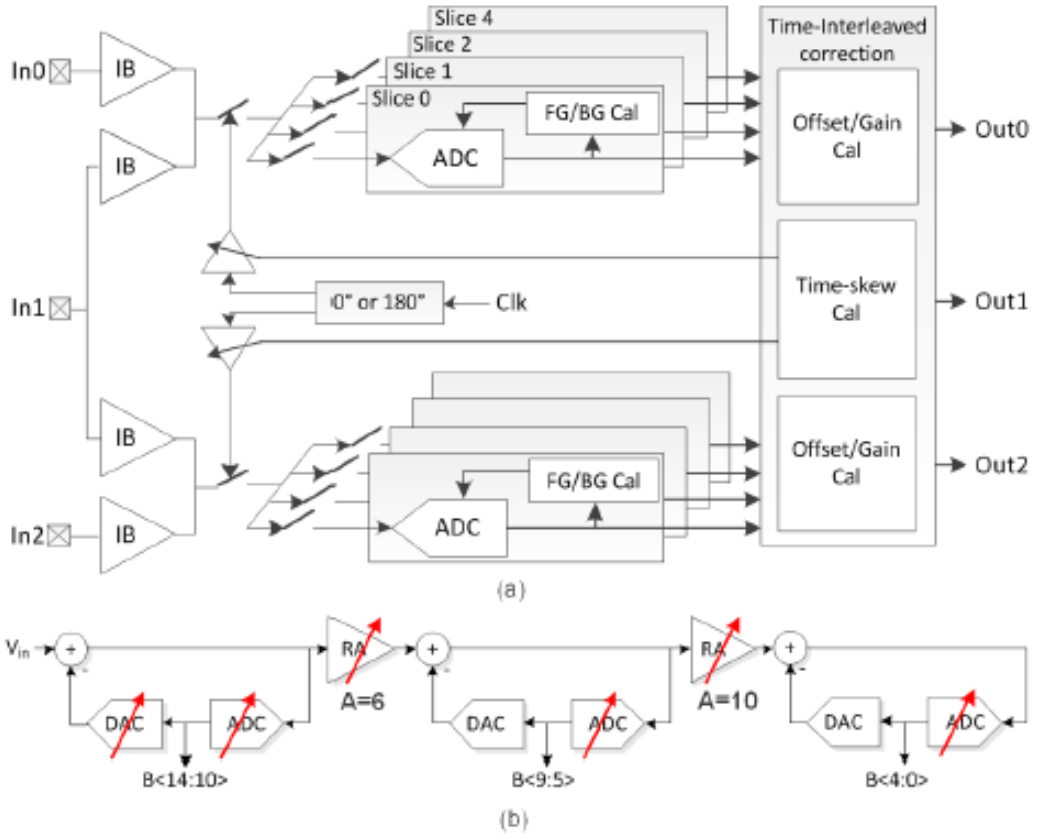


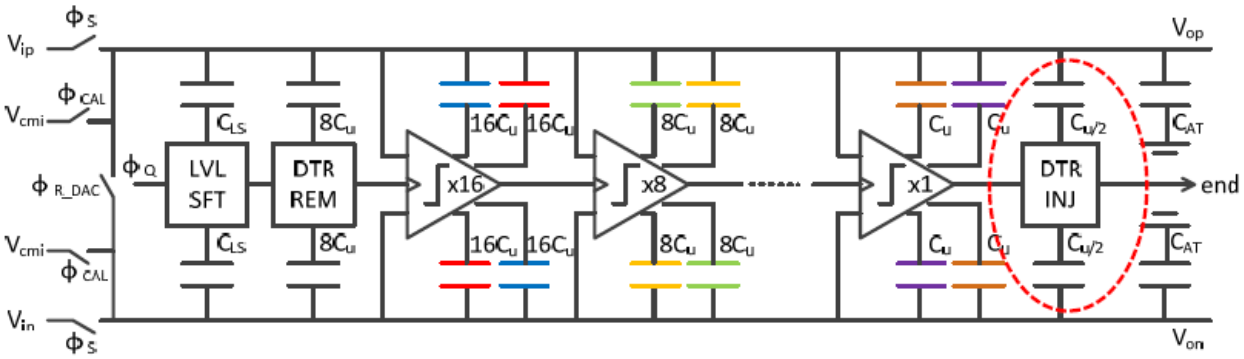
Figure 16.1.1: Block diagrams: (a) time-interleaved ADC; (b) three-stage asynchronous pipelined-SAR.

See, e.g., Vaz White Paper, 277. The Accused RFSoC Products' analog-to-digital converters are 13-bit converters with a 3-stage pipelined successive approximation register (SAR) architecture, where each stage has 5 bits, thereby providing redundancy. *See, e.g.*, Vaz White Paper, 276.

44. The Accused RFSoC Products' analog-to-digital converters have two analog-to-digital units, each analog-to-digital unit consisting of four sub-ADC slices and a sampling network with a front-end switch and four channel switches. *See, e.g.*, Vaz White Paper, 276 ("Each 2GS/S ADC unit consists of four interleaved 500 MS/s sub-ADC slices and a sampling network composed of a front-end switch and four channel switches used to interleave the four ADC slices without time-skew calibration requirements."); *id.* ("Fig. 16.1.1b shows the topology of each sub-ADC. It uses three asynchronous 5b SAR stages separated by two residue amplifiers

(RA). For speed reasons, each stage uses a split-capacitor MDAC to maintain constant common mode and five cascaded dynamic comparators.").

45. The Accused RFSoC Products' analog-to-digital converters have a dither device for applying a dither to the conversion engine. For example, the first and second stages in a sub-ADC slice use dithering injecting capacitors to apply dither to the conversion engine:



See, e.g., Xilinx ISSCC Presentation, slide 21.

46. The Accused RFSoC Products' analog-to-digital converters have a controller adapted to operate the conversion engine to perform a successive approximation conversion of an analog input. For example, the Accused RFSoC Products' analog-to-digital converters include a controller that provides control signals (e.g., convert, clear) for each successive approximation register (SAR) stage in the sub-ADC slice:

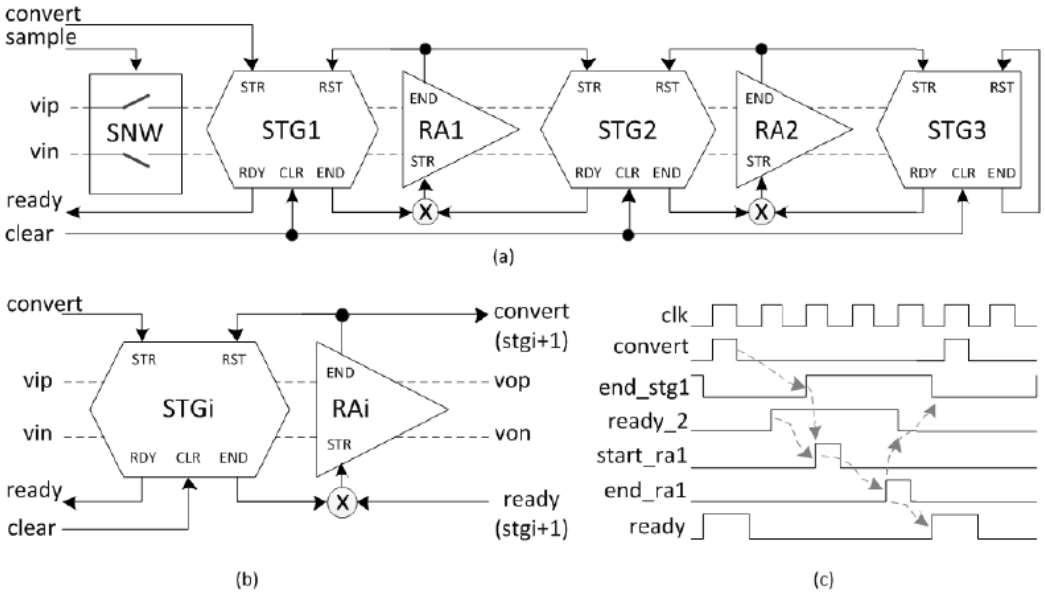
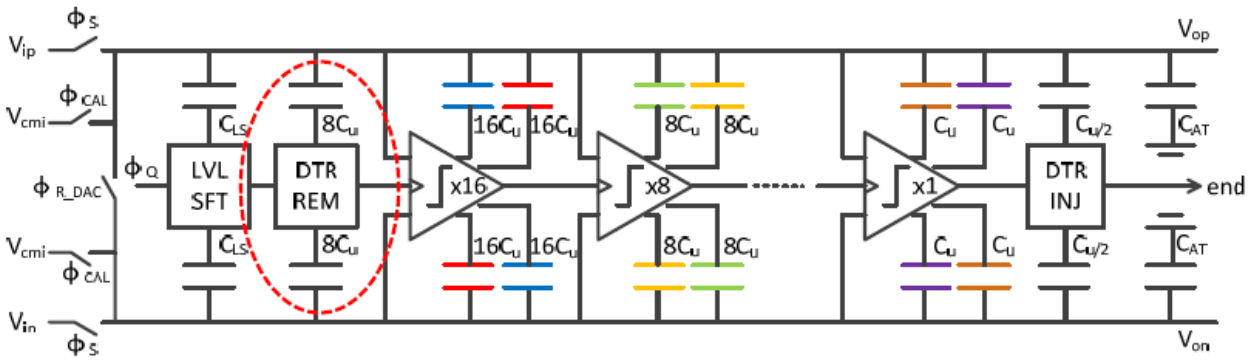


Figure 16.1.2: (a) Clock interface (b) Inter-stage block diagram (c) Inter-stage timing diagram.

See, e.g., Vaz White Paper, 277.

47. In the Accused RFSoC Products' analog-to-digital converters the dither is removed from the conversion engine prior to completion of successive approximation bit trials as part of the analog-to-digital conversion. For example, the second and third stages in the sub-ADC slice use dithering removing capacitors that remove dither before completion of the analog-to-digital conversion:



See, e.g., Xilinx ISSCC Presentation, slide 20.

48. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the ’518 Patent, at least by its customers’ use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the ’518 patent and its infringement of the ’518 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx’s inducement of infringement of the ’518 Patent has been done with specific intent to infringe that patent.

49. Xilinx’s infringement of the ’518 Patent has been willful and its ongoing infringement of the ’518 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI’s notice, knowing that such products would infringe the ’518 Patent.

50. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx’s infringement of the ’518 Patent.

COUNT III
(Infringement of U.S. Patent No. 6,900,750)

51. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

52. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the ’750 Patent, including at least claim 19, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

53. The Accused RFSoC Products adjust an offset signal in a signal conditioning system. For example, the RFSoC analog-to-digital converters include an analog-to-digital converter with a 3-stage pipelined successive approximation register (SAR) architecture, where the stages are separated by residue amplifiers:

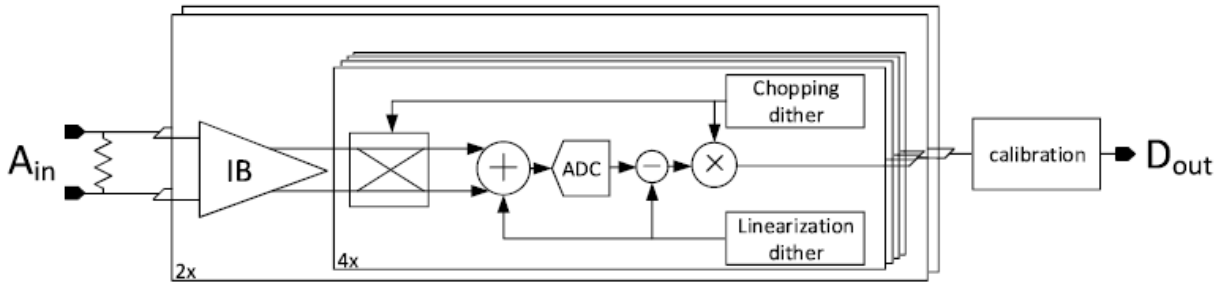


Fig.4. Simplified ADC architecture.

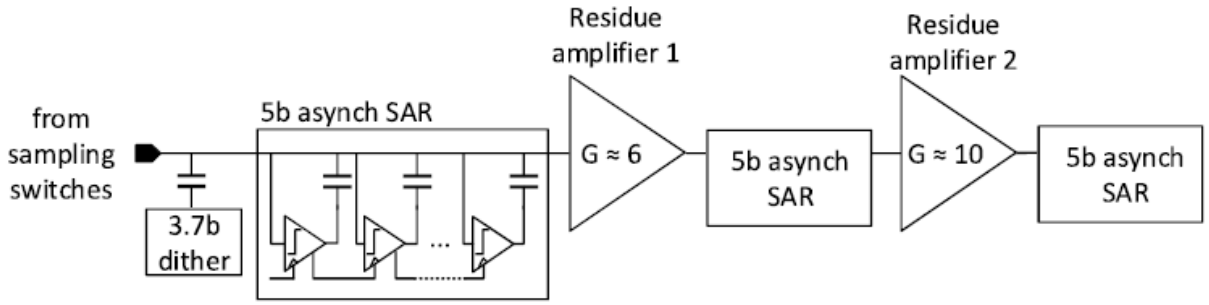


Fig.7. Simplified ADC channel.

Verbruggen White Paper, Figs. 4, 7.

54. The Accused RFSoC Products' analog-to-digital converters clock a first converter with a random clock. For example, the Accused RFSoC Products' analog-to-digital converters have an analog-to-digital converter with the 3-stage pipelined successive approximation register (SAR) architecture. *See, e.g.*, Verbruggen White Paper, Fig. 4. The Accused RFSoC Products' analog-to-digital converters also include a 1-bit pseudo-random bit sequence (i.e., a random clock) to control chopping of the input signal to the analog-to-digital converter.

55. The Accused RFSoC Products' analog-to-digital converters sense a first offset signal of the first converter. For example, the Accused RFSoC Products' analog-to-digital

converters include offset calibration loops that measure and correct the average of each channel output of the analog-to-digital converter. The Accused RFSoC Products' analog-to-digital converters include an offset calibration block inside the chopping path (OCB1) and an offset calibration block outside the chopping path (OCB2):

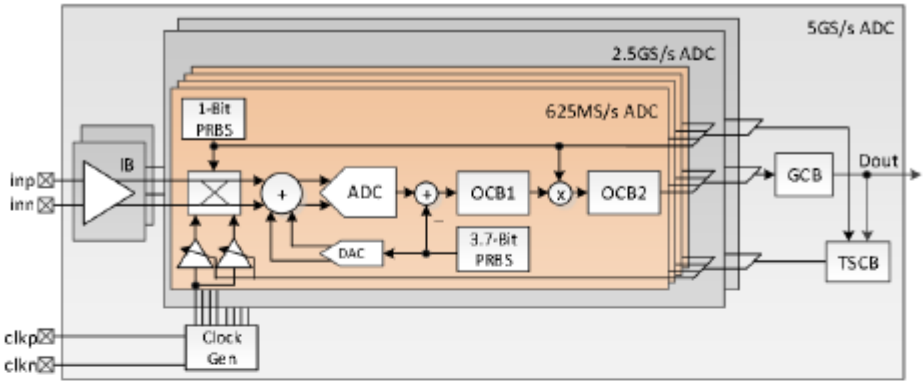


Fig. 1 ADC architecture.

The figure also shows the detail of the TI calibration blocks. A first offset calibration block (OCB1) is placed inside the chopping path. This block has the ability to remove the offset of the ADC block without being affected by the input signal characteristics. This prevents the channel offset from being spread over the output spectrum after the un-chopping multiplier. Hence, only the flicker noise of the ADC gets spread across the spectrum which minimizes the noise penalty.

For further performance optimization, the offset mismatch of the chopping switches, which is not seen by OCB1, is cancelled by OCB2 placed after the un-chopping multiplier. This block runs in the foreground at start-up to extract the offset difference between switches and is frozen during normal operation to avoid any interaction with the input signal characteristics.

See, e.g., Vaz VLSI Paper, 99.

56. The Accused RFSoC Products' analog-to-digital converters condition one of an input signal and an output signal of the first converter with the first offset signal. For example,

the first offset sensor includes two loops; one offset calibration loop is active inside the chopping and the second offset calibration loop is acting outside the chopping:

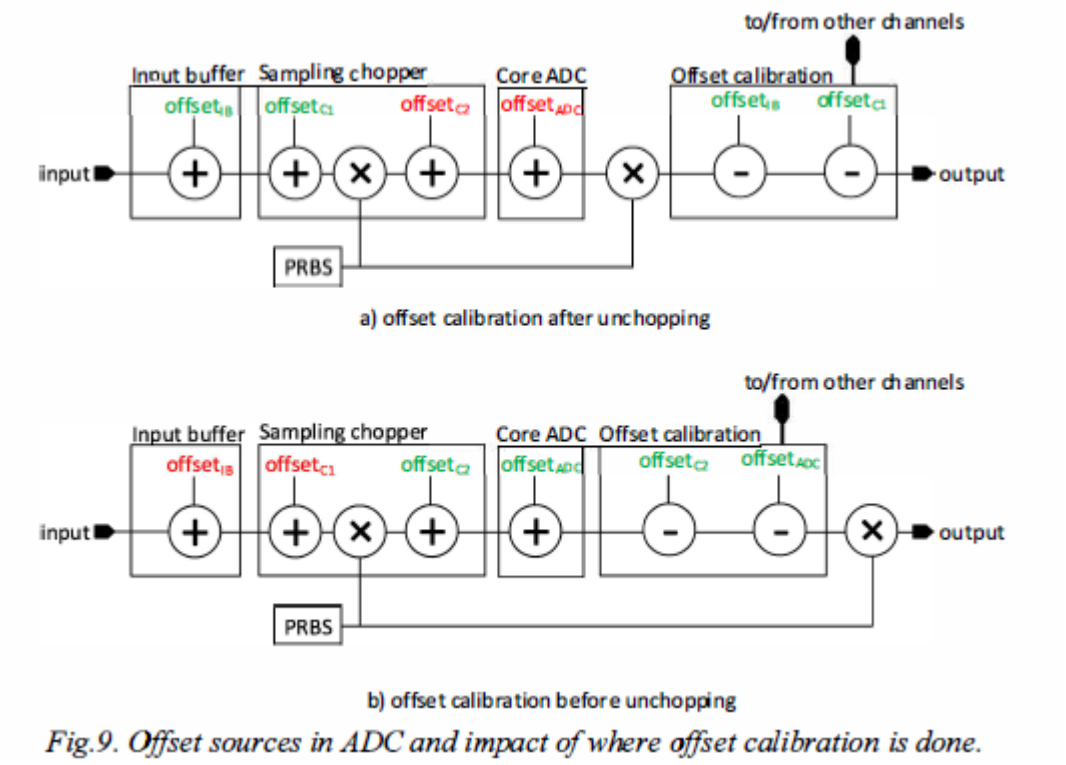


Fig.9. Offset sources in ADC and impact of where offset calibration is done.

See, e.g., Verbruggen White Paper, Fig. 9.

57. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the '750 Patent, at least by its customers' use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the '750 patent and its infringement of the '750 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx's inducement of infringement of the '750 Patent has been done with specific intent to infringe that patent.

58. Xilinx's infringement of the '750 Patent has been willful and its ongoing infringement of the '750 Patent continues to be willful. Xilinx has chosen to manufacture and

sell the Accused RFSoC Products, even after ADI's notice, knowing that such products would infringe the '750 Patent.

59. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx's infringement of the '750 Patent.

COUNT IV
(Infringement of U.S. Patent No. 10,250,250)

60. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

61. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the '250 Patent, including at least claim 1, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

62. Xilinx's Accused RFSoC Products include an analog-to-digital converter with a bootstrapped switching circuit for accelerated turn on. For example, the Accused RFSoC Products include four "bootstrapped switches" (BS), acting as sampling switches, in the analog-to-digital converter's "sampling network":

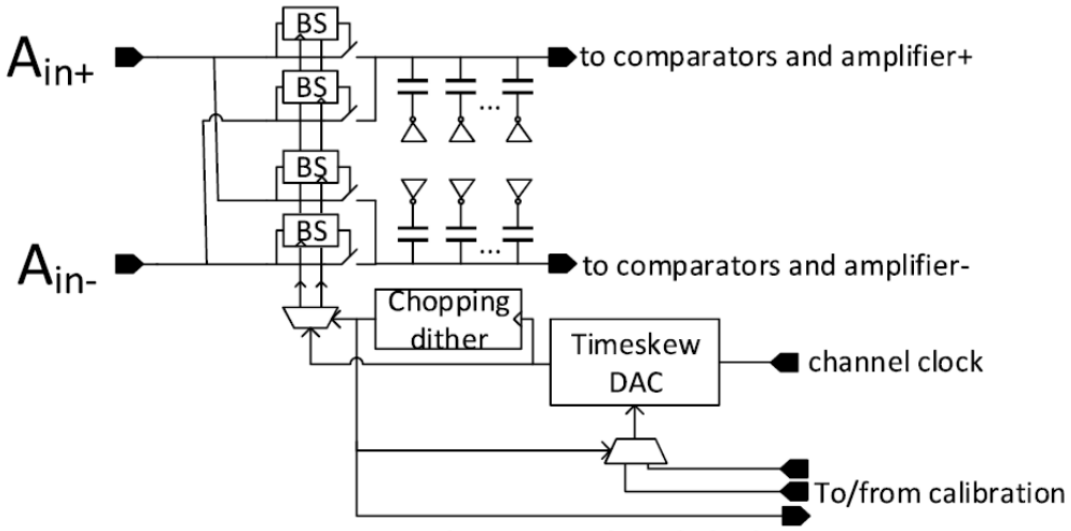


Fig.6. Sampling network and clocking

See, e.g., Verbruggen White Paper, at Fig. 6 and 97-98 (confirming RFSOC includes four sampling switches which are bootstrapped).

63. The Accused RFSoC Products include four sampling switches as bootstrapped switching circuits. Each sampling switch receives a voltage input signal and a gate voltage. For example, the sampling switch receives a voltage input signal on a source, in which the gate is controlled by an output of a bootstrapped voltage generator, which generates a boosted voltage based on the voltage input signal. The sampling switch is implemented as a MOS transistor. *See, e.g.*, Verbruggen White Paper, at 97-98, Fig. 6.

64. The bootstrapped switching circuit in the Accused RFSoC Products includes the bootstrapped voltage generator comprising a positive feedback loop, which is activated by a clock signal, to generate a gate voltage for turning on the sampling switch. For example, a bootstrapped voltage generator portion of the bootstrapped switching circuit generates the gate voltage for the sampling switch in the sampling network shown above. *Id.*

65. The bootstrapped voltage generator portion's positive feedback loop includes an output transistor to output the gate voltage of the sampling switch and an input transistor to

receive the voltage input signal and to be driven by the gate voltage as positive feedback. For example, the output transistor is implemented as a MOS transistor that couples a first node of a voltage storing capacitor to a gate of the sampling switch. The input transistor is implemented as a MOS transistor that couples the input signal to another node of the voltage storing capacitor, and its gate is driven by the same gate signal that drives the gate of the sampling switch.

66. The bootstrapped switching circuit in the Accused RFSoC Products includes a jump start circuit to turn on the output transistor and to cease turning on the output transistor after a limited period of time during a startup of the positive feedback loop to allow the positive feedback loop to continue assisting the output transistor in generating the gate voltage for turning on the sampling switch. For example, the bootstrapped switching circuit includes a transistor network to process clock signals to form a delayed, shortened clock signal so as to turn on the output transistor but also cease turning on the output transistor after a limited time as a result of the signal shape of the delayed, shortened clock signal. In doing so, the transistor network allows the positive feedback loop to continue assisting the output transistor in generating the gate voltage to turn on the sampling switch.

67. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the ’250 Patent, at least by its customers’ use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the ’250 patent and its infringement of the ’250 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx’s inducement of infringement of the ’250 Patent has been done with specific intent to infringe that patent.

68. Xilinx's infringement of the '250 Patent has been willful and its ongoing infringement of the '250 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI's notice, knowing that such products would infringe the '250 Patent.

69. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx's infringement of the '250 Patent.

COUNT V
(Infringement of U.S. Patent No. 7,274,321)

70. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

71. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the '321 Patent, including at least claim 1, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

72. The Accused RFSoC Products include multiple analog-to-digital converters. For example:

Key Components of the Zynq UltraScale+ RFSoC

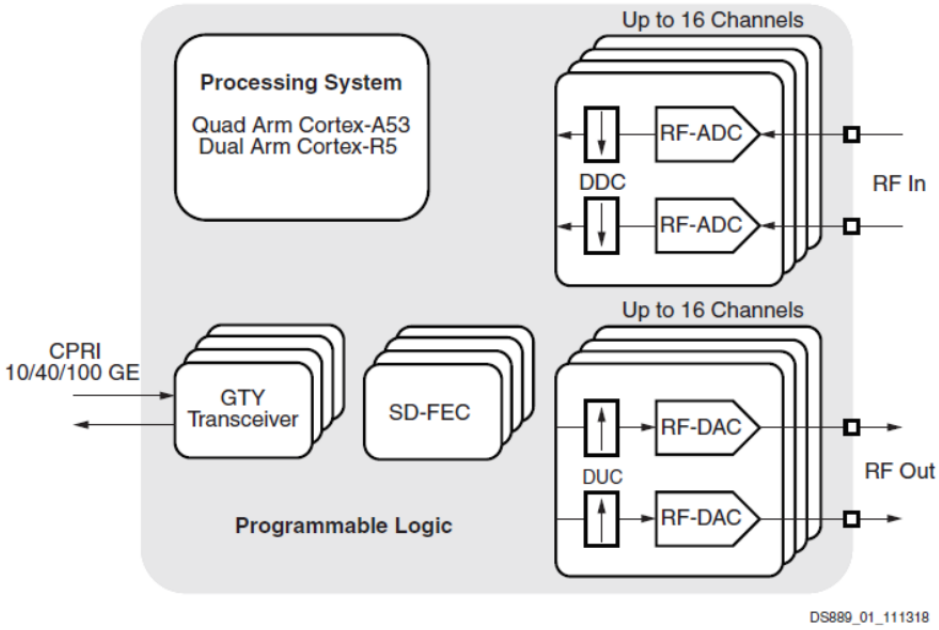


Figure 1: **Zynq UltraScale+ RFSoC**

See, e.g., RFSoC Data Sheet, 2.

73. The Accused RFSoC Products' analog-to-digital converters include an input for receiving an input signal to be digitized, and a first converter core for performing a first part of an analog-to-digital conversion, said first converter core comprising at least three switched capacitor analog-to-digital conversion engines operating in parallel and in a co-operative manner and for outputting a first digital result and an analog representation of the first digital result. For example, the Accused RFSoC Products have a pipelined architecture, with three pipelined 5-bit successive approximation register (SAR) ADCs being the three converter cores:

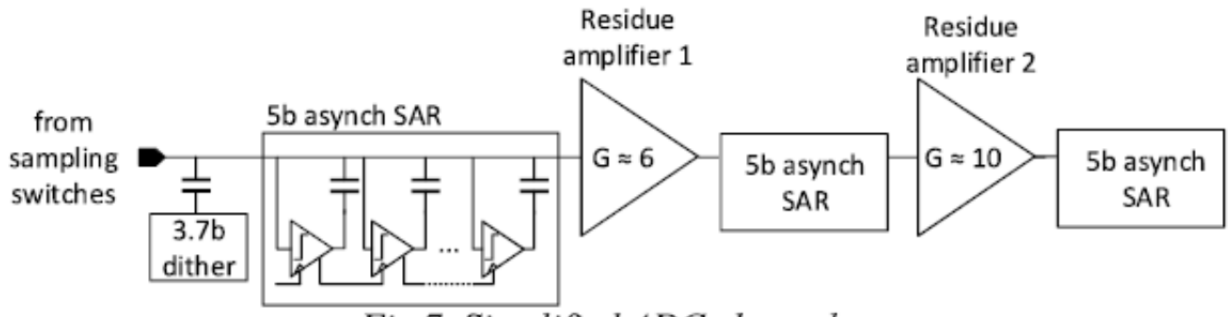
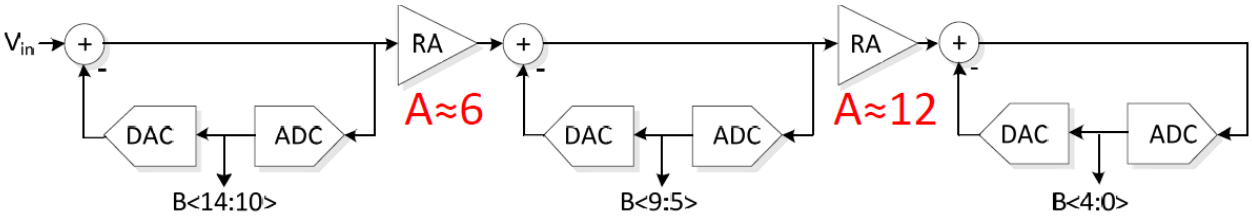


Fig. 7. Simplified ADC channel.

See, e.g., Verbruggen White Paper, Fig. 7.

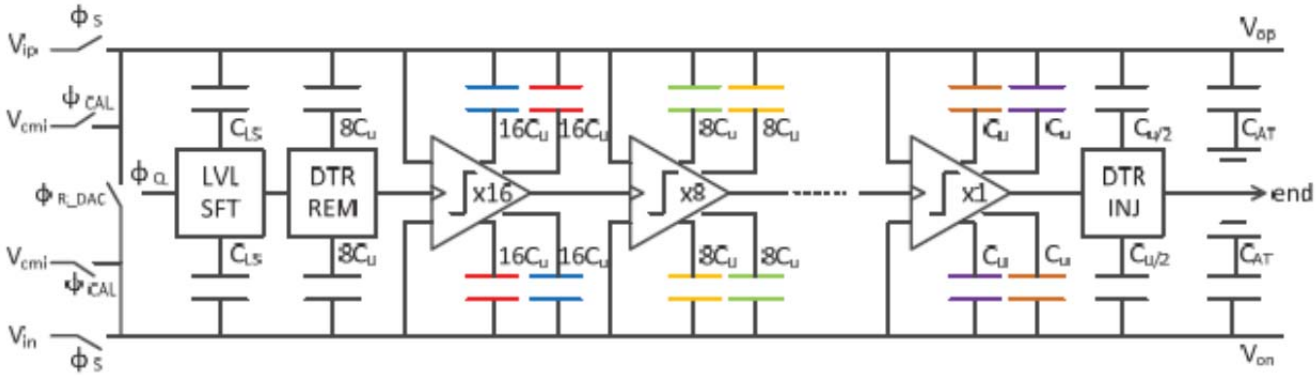


See, e.g. Xilinx ISSCC Presentation, slide 11.

74. The first converter core, *i.e.*, a first 5-bit SAR ADC, receives an input signal to be digitized (for example, V_{in}). The first converter core performs a first part of the analog-to-digital conversion and yields a 5-bit digital result (for example, B<14:10>), and its analog representation (for example, DAC output). In addition, the Accused RFSoC Products have two analog-to-digital units, each analog-to-digital unit having four sub-ADC slices and a sampling network with a front-end switch and four channel switches for interleaving the slices. *See, e.g.*, Vaz White Paper, 276 ("Each 2GS/S ADC unit consists of four interleaved 500 MS/s sub-ADC slices and a sampling network composed of a front-end switch and four channel switches used to interleave the four ADC slices without time-skew calibration requirements."). Each slice has three converter cores that provide bits B<14:10>, B<9:5>, and B<4:0>.

75. The first converter core includes at least three switched capacitor analog-to-digital conversion engines operating in parallel and in a co-operative manner. For example, the first

converter core includes three 5-bit asynchronous SAR ADCs. *See, e.g.*, Verbruggen White Paper, Fig. 7. The first converter core includes five switched capacitor analog-to-digital conversion engines (x16, x8, …, x1). For example:



See, e.g., Xilinx ISSCC Presentation, slide 15.

76. The Accused RFSoC Products' analog-to-digital converters include a first residue generator that generates a first residue as a difference between the input signal and the analog representation of the first digital result. For example, the output of the DAC is subtracted from the analog Vin, and similar operations are performed at the other two converter cores. *See, e.g.*, Xilinx ISSCC Presentation, slide 11.

77. The Accused RFSoC Products' analog-to-digital converters include a second converter core for performing a second part of the analog-to-digital conversion by converting the first residue. For example, the second converter core (for example, the second 5-bit SAR ADC) receives the residue from the first converter core (for example, the signal from Residue Amplifier 1) and performs a second part of the conversion (for example, B<9:5>). For example:

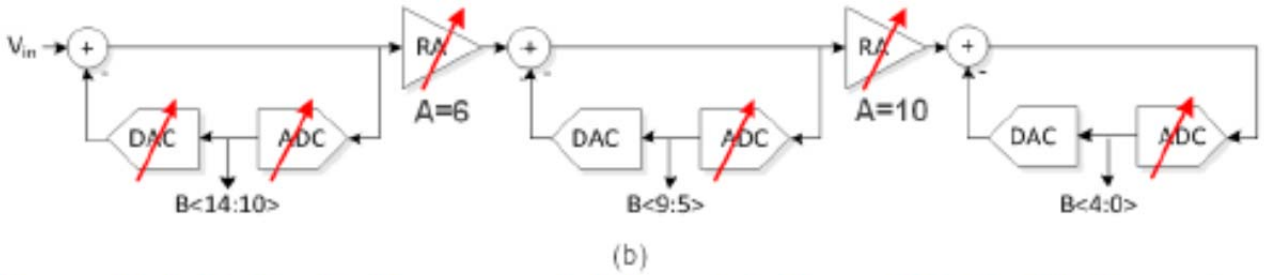
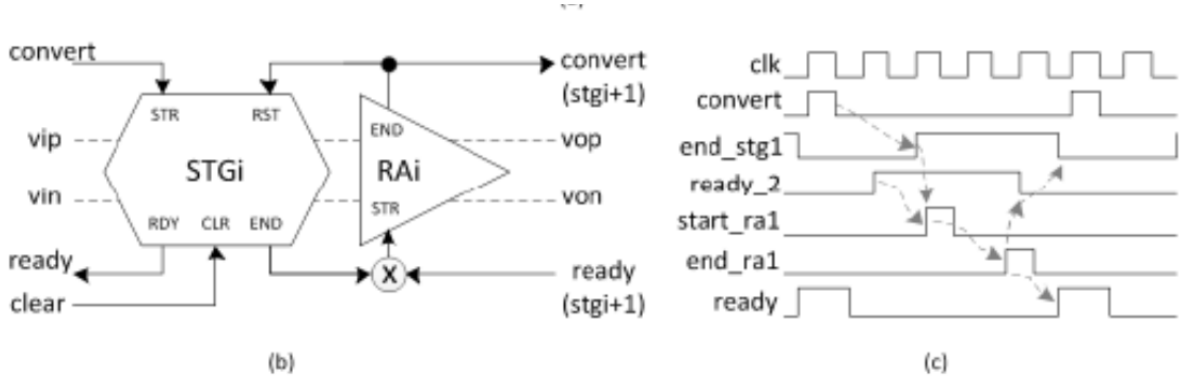


Figure 16.1.1: Block diagrams: (a) time-interleaved ADC; (b) three-stage asynchronous pipelined-SAR.

See, e.g., Vaz White Paper, 277; *see also* Verbruggen White Paper, Fig. 7.

78. The Accused RFSoC Products' analog-to-digital converters also include a controller for controlling the operation of the engines such that the engines co-operate to perform a successive approximation search, and the first converter core is further operable to act as the first residue generator. For example, the analog-to-digital controller uses numerous controls so that the converter cores and engines (including, for example, STGi) co-operate to perform a successive approximation search:



Vaz White Paper, 2017, Fig. 16.1.2. The first converter core (for example, the first 5-bit SAR) operates to subtract the analog representation produced by STG1 from the original analog input signal to produce a residue signal and provide the residue signal to Residue Amplifier 1. *See, e.g.*, Verbruggen White Paper, Fig. 7.

79. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the ’321 Patent, at least by its customers’ use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the ’321 patent and its infringement of the ’321 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx’s inducement of infringement of the ’321 Patent has been done with specific intent to infringe that patent.

80. Xilinx’s infringement of the ’321 Patent has been willful and its ongoing infringement of the ’321 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI’s notice, knowing that such products would infringe the ’321 Patent.

81. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx’s infringement of the ’321 Patent.

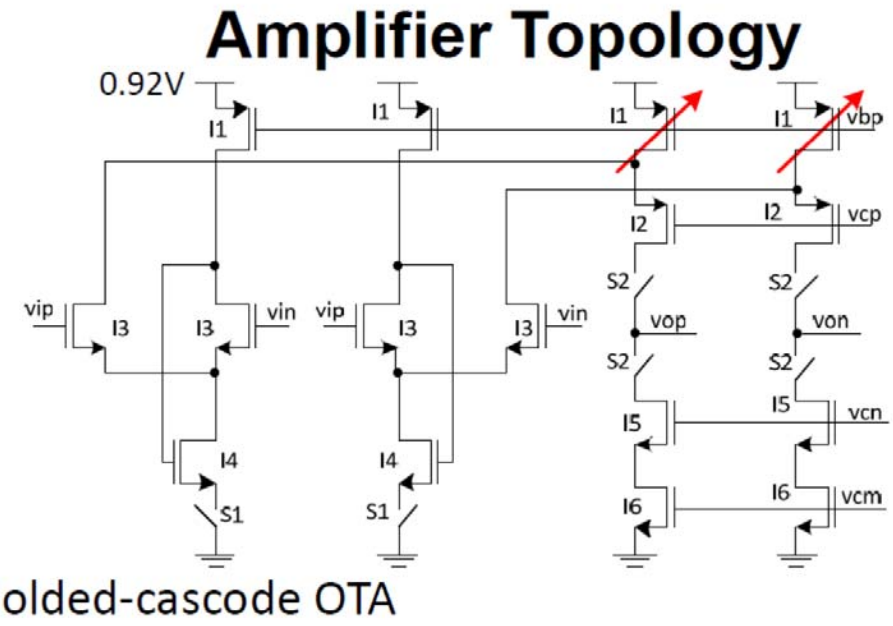
COUNT VI
(Infringement of U.S. Patent No. 7,012,463)

82. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

83. Xilinx has infringed and continues to infringe, directly and/or indirectly, one or more claims of the ’463 Patent, including at least claim 11, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

84. The Accused RFSoC Products are integrated circuits. *See, e.g.*, RFSoC Data Sheet, 1.

85. The Accused RFSoC Products include a differential amplifier circuit with an output portion and a current sinking portion. The output portion includes dual outputs that provide an average output level. For example, the Accused RFSoC Products include residue amplifiers that have a folded-cascode operational transconductance amplifier (OTA) topology:



See, e.g., Xilinx ISSCC Presentation, slide 23. Each residue amplifier has an output portion with dual outputs (for example, von and vop) and a current sinking portion (for example, I5 and I6).

86. The Accused RFSoC Products include a common-mode feedback circuit coupled to the output portion of the differential amplifier circuit. In the Accused RFSoC Products' circuit, the feedback circuit provides a desired common-mode level in a first operational mode. In a second operational mode, the feedback circuit generates a feedback signal proportional to the difference between the average output level and the desired common-mode level, and the feedback signal is coupled to the current sinking portion. For example, the amplifier includes a first transistor network to provide desired common mode level signals when the transistors are activated by a first clock signal. The transistor network allows a first set of capacitors to sample

a pair of supply voltages (for example, V_{DD} and V_{SS}). In response to another clock signal, a second transistor network is activated which connects the first set of capacitors with a second set of capacitors. Consequently, charge is redistributed among the capacitors to generate a feedback signal that is proportional to the difference between the average output level and the desired common-mode level.

87. The feedback signal generated by the feedback circuit is coupled to the current sinking portion of the differential amplifier circuit.

88. The Accused RFSoC Products include an impedance matching circuit connected to the precharging capacitor of the feedback circuit to adjust the feedback signal. For example, as described above, the Accused RFSoC Products include an impedance matching circuit coupled to a bias level coupled to at least the first set of capacitors.

89. In the Accused RFSoC Products, the desired common-mode signal is provided to a precharging capacitor in the first operational mode, the precharging capacitor including a terminal coupled to the impedance matching circuit. For example, as described above, the first set of capacitors are precharging capacitors, and are coupled to the impedance matching circuit.

90. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the ’463 Patent, at least by its customers’ use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the ’463 patent and its infringement of the ’463 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx’s inducement of infringement of the ’463 Patent has been done with specific intent to infringe that patent.

91. Xilinx's infringement of the '463 Patent has been willful and its ongoing infringement of the '463 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI's notice, knowing that such products would infringe the '463 Patent.

92. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx's infringement of the '463 Patent.

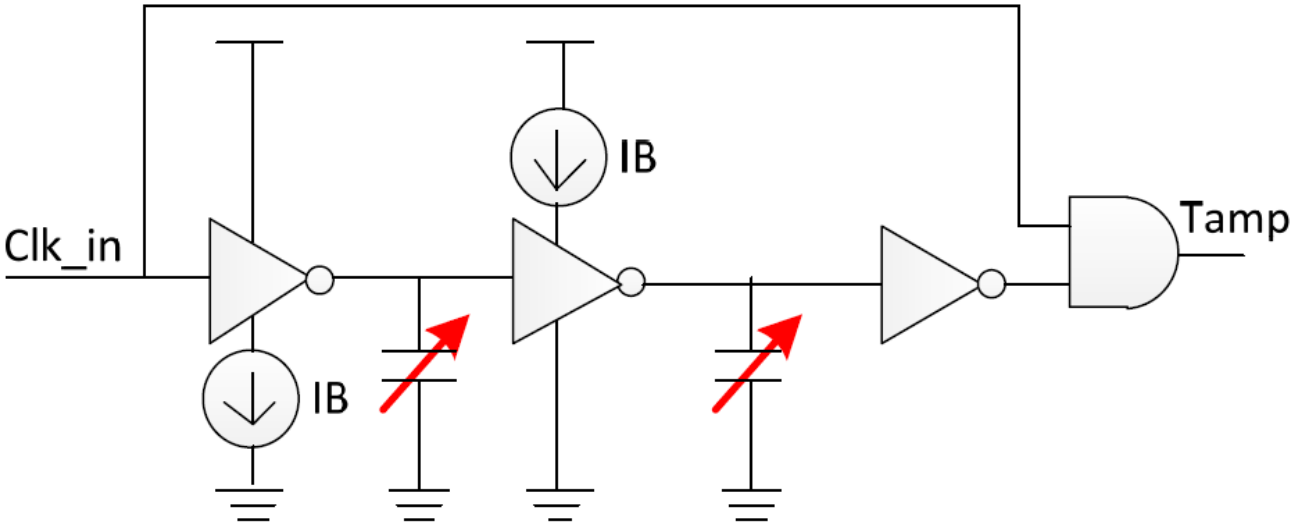
COUNT VII
(Infringement of U.S. Patent No. 8,487,659)

93. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

94. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the '659 Patent, including at least claim 9, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

95. The Accused RFSoC Products control PVT effects in a circuit system. For example, the Accused RFSoC Products include a residue amplifier and an integration time calibration circuit for controlling amplification time in the residue amplifier. The integration time calibration circuit is an integrated circuit. *See* Vaz White Paper, 276-277. As further detailed below, these components control PVT effects in the circuit system.

96. The integration time calibration circuits in the Accused RFSoC Products each charge a capacitive element with reference to a first supply voltage in response to a state change in an input signal. For example, the integration time calibration circuits include a delay generator circuit:



See, *e.g.*, Xilinx ISSCC Presentation, slide 24. The delay generator circuit includes a chain of three inverters with variable capacitors at the output of the first two inverters. The delay generator circuit receives a clock signal (for example, Clk_in) at the input of the first inverter. In response to a state change in the clock signal (for example, the rising or falling edge of Clk_in), each of the variable capacitors is charged with reference to a respective supply voltage (for example, a V_{DD} or V_{SS}, which could be ground).

97. The integration time calibration circuits in the Accused RFSoC Products generate an output voltage when the capacitive element's output voltage reaches a voltage threshold. For example, when the voltage across each of the variable capacitors reaches a voltage threshold associated with the next inverter in the chain of inverters, the state of inverter switches, generating a new output voltage. *See, e.g.,* Xilinx ISSCC Presentation, slide 24. At the end of the inverter chain, the output from the delay generator circuit is combined with the original clock signal through an AND gate to generate a timing signal (for example, Tamp).

98. The Accused RFSoC Products are integrated circuits, and the delays between the state change of the input signal and the generated output voltage vary inversely in response to

PVT effects on other components of the integrated circuit. On information and belief, the Accused RFSoC Products use at least clock control and capacitive elements to account for PVT effects, providing the recited inverse relationship. For example, in the Accused RFSoC Products "[a] single RA design is used to reduce design/verification effort, with only a minor penalty to power consumption. The gain of the integrating RA is adjusted by appropriately sizing its load capacitance. The FG calibration corrects comparator offsets, RA offset and gain and capacitor mismatch [i.e., process]. The BG calibration adjusts the RA gain and comparator offset drift due to temperature and voltage variations during operation. … Figure 16.1.2a details the clock interface of the pipelined-SAR ADC. The integration time of the RAs varies considerably across PVT, and leakage limits the achievable performance of the ADC at low sampling frequencies if using a synchronous clocking scheme." *See* Vaz White Paper, 276.

99. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the '659 Patent, at least by its customers' use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the '659 patent and its infringement of the '659 patent since at least July 31, 2019, when ADI provided Xilinx with claim charts substantiating its infringement of the patent. Xilinx's inducement of infringement of the '659 Patent has been done with specific intent to infringe that patent.

100. Xilinx's infringement of the '659 Patent has been willful and its ongoing infringement of the '659 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI's notice, knowing that such products would infringe the '659 Patent.

101. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx's infringement of the '659 Patent.

COUNT VIII
(Infringement of U.S. Patent No. 7,286,075)

102. ADI incorporates the allegations contained in the preceding paragraphs as if fully set forth herein.

103. Xilinx has infringed and continues to infringe, directly and/or indirectly, literally and/or equivalently, one or more claims of the '075 Patent, including at least claim 16, by making, using, selling, offering for sale in, and/or importing into, the United States certain products with analog-to-digital conversion technology, including at least the Accused RFSoC Products.

104. The Accused RFSoC Products include an analog-to-digital converter system to convert an analog input signal to a digital code. For example:

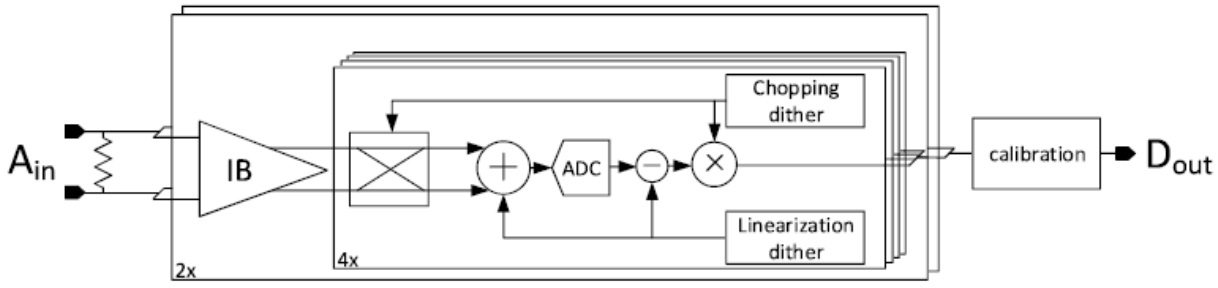


Fig.4. Simplified ADC architecture.

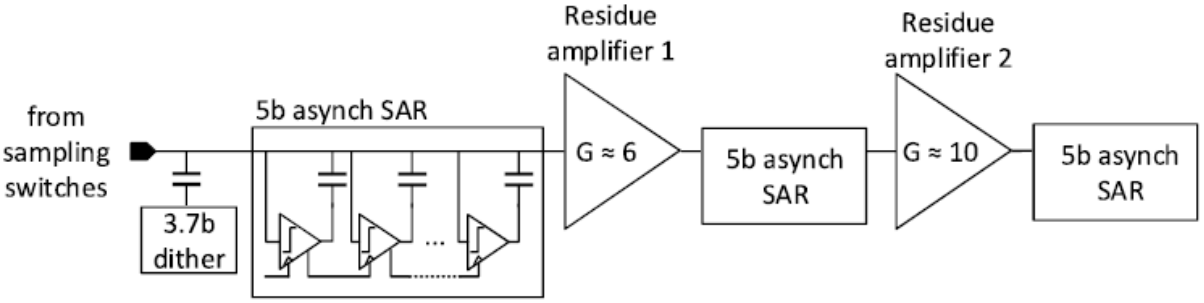


Fig.7. Simplified ADC channel.

See, e.g., Verbruggen White Paper, Figs. 4 & 7.

105. The Accused RFSoC Products' analog-to-digital converter system has a switch capacitor array to provide samples of said analog input signal and convert samples to a digital signal. For example, the Accused RFSoC Products' analog-to-digital converter system has a "sampling switches" that provides samples of the analog input signal:

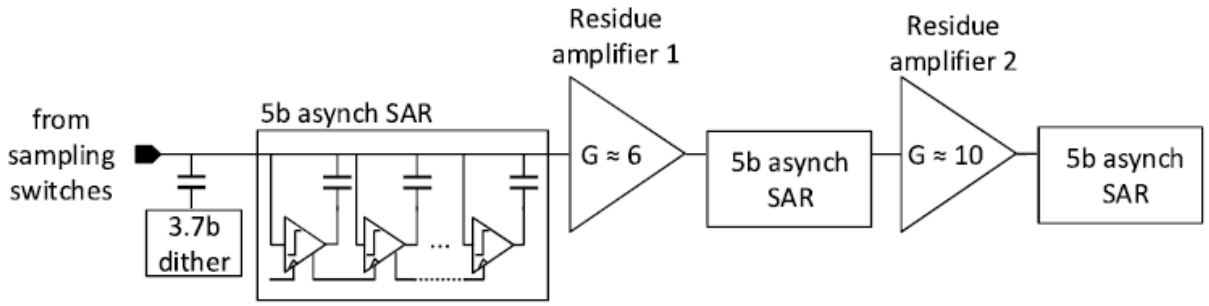


Fig. 7. Simplified ADC channel.

See, e.g., Verbruggen White Paper, Fig. 7.

106. The Accused RFSoC Products' analog-to-digital converter system has a switched capacitor digital to analog converter responsive to a control word, wherein after sampling a dither signal is injected onto the switched capacitor array to make a known perturbation to the charge stored on the array. For example, the Accused RFSoC Products' analog-to-digital converter system has digital-to-analog converters that receive a 3.7-bit pseudo-random bit sequence and inject analog dither signals at an input of an analog-to-digital converter:

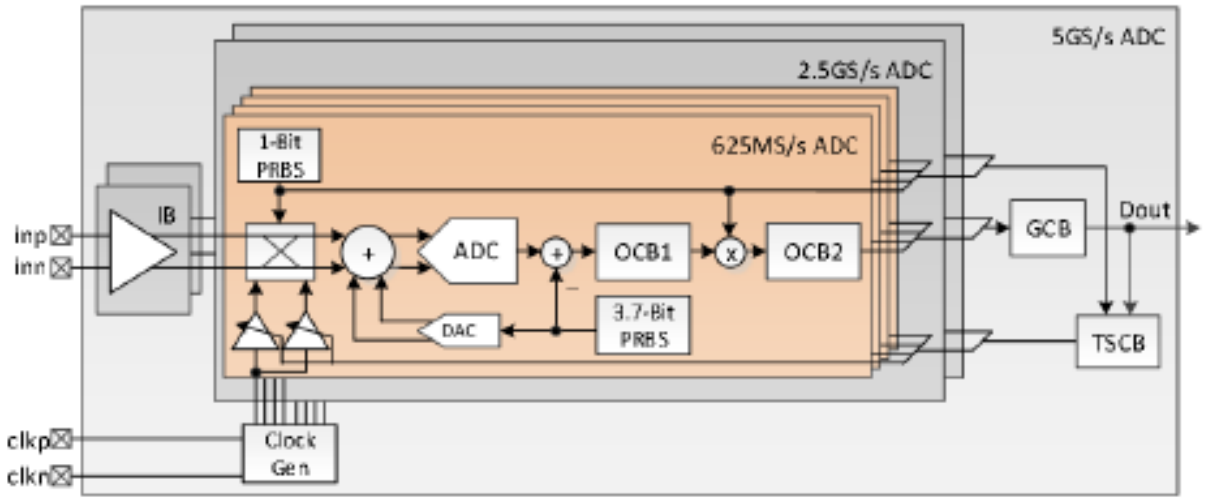


Fig. 1 ADC architecture.

See, e.g., Vaz VLSI Paper, 99; *see also* Verbruggen White Paper, Fig. 7 & 98 ("These errors are randomized by injecting a 3.7b PRBS dither signal just after sampling.").

107. Xilinx has actively and knowingly induced, and is continuing to actively and knowingly induce, infringement of the '075 Patent, at least by its customers' use of the Accused RFSoC Products. For example, on information and belief, Xilinx instructs its customers by way of manuals or product documentation to infringe the asserted claims by using the Accused RFSoC Products. Xilinx has had knowledge of the '075 patent and its infringement of the '075 patent since at least the filing of this complaint. Xilinx's inducement of infringement of the '075 Patent has been done with specific intent to infringe that patent.

108. Xilinx's infringement of the '075 Patent has been willful and its ongoing infringement of the '075 Patent continues to be willful. Xilinx has chosen to manufacture and sell the Accused RFSoC Products, even after ADI's notice, knowing that such products would infringe the '075 Patent.

109. ADI has been and is being irreparably harmed, and has incurred and will continue to incur damages, as a result of Xilinx's infringement of the '075 Patent.

REQUEST FOR RELIEF

WHEREFORE, Plaintiff ADI respectfully requests that this Court enter judgment as follows:

a. Declaring that Xilinx has infringed the ’452, ’518, ’750, ’250, ’321, ’463, ’659, and ’075 Patents;

b. Granting a permanent injunction, enjoining Xilinx and its officers, agents, servants, employees, attorneys, and all other persons acting in concert or participation with them, from further infringement of the ’452, ’518, ’750, ’250, ’321, ’463, ’659, and ’075 Patents, including but not limited to the suspension of its Accused RFSoC product line and any further development of the Accused RFSoC product line;

c. Awarding ADI damages adequate to compensate it for Xilinx’s infringing activities, including supplemental damages for any post-verdict infringement up until entry of the final judgment with an accounting as needed, together with pre-judgment and post-judgment interest on the damages awarded;

d. Finding Xilinx’s infringement to be willful and awarding enhanced damages in an amount up to treble the amount of compensatory damages as justified under 35 U.S.C. § 284;

d. Finding this to be an exceptional case and awarding ADI its attorneys’ fees and costs; and

e. Awarding ADI any such other and further relief as the Court deems just and proper.

JURY DEMAND

ADI hereby demands a trial by jury on all issues so triable.

MORRIS, NICHOLS, ARSHT & TUNNELL LLP

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