IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ANALOG DEVICES, INC., Plaintiff, v. XILINX, INC., Defendant.	)	C.A. No. 19-2225-RGA **DEMAND FOR JURY TRIAL**
XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD., Counterclaim Plaintiffs, v. ANALOG DEVICES, INC., Counterclaim Defendant.	)	

ANSWER TO COMPLAINT, AFFIRMATIVE DEFENSES, AND COUNTERCLAIMS

Defendant Xilinx, Inc., by and through its undersigned counsel, hereby responds to the Complaint filed by Analog Devices, Inc. ("ADI") by admitting, denying, and alleging as set forth below. Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively, "Xilinx") also submit Counterclaims against ADI.

INTRODUCTION[1]

1. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 1 of the Complaint and therefore denies the allegations.

2. Xilinx, Inc. denies the allegations in Paragraph 2 of the Complaint.

[1] For convenience and clarity, Xilinx, Inc.'s Answer uses the same headings as set forth in the Complaint. In so doing, Xilinx, Inc. does not admit any of the allegations contained in ADI's headings.

PARTIES

3. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 3 of the Complaint and therefore denies the allegations.

4. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 4 of the Complaint and therefore denies the allegations.

5. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 5 of the Complaint and therefore denies the allegations.

6. Xilinx, Inc. admits that it is a Delaware corporation, with a principal business address of 2100 Logic Drive, San Jose, California 95124.

JURISDICTION AND VENUE

7. Xilinx, Inc. admits that this Complaint purports to state an action under the patent laws of the United States and that this Court has subject matter jurisdiction over ADI's claims, as set forth in the Complaint, pursuant to 28 U.S.C. §§ 1331 and 1338.

8. Xilinx, Inc. admits that this Court has personal jurisdiction over Xilinx, Inc., and that Xilinx, Inc. is a Delaware corporation. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations in Paragraph 8 of the Complaint.

9. Xilinx, Inc. admits that it is a Delaware corporation and does not contest that venue is proper in this District.

FACTUAL ALLEGATIONS

ADI's Patented Technologies

10. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 10 of the Complaint and therefore denies the allegations.

11. Xilinx, Inc. admits that the Complaint asserts eight patents that purport to relate to analog-to-digital converters. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations in Paragraph 11 of the Complaint.

12. Xilinx, Inc. admits that the cover of United States Patent No. 7,719,452 (the "'452 Patent") is titled "Pipelined Converter Systems With Enhanced Linearity" and states that it was issued on May 18, 2010. Xilinx, Inc. admits that a copy of what appears to be the '452 Patent is attached as Exhibit A to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 12 of the Complaint regarding ownership of the '452 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 12 of the Complaint.

13. Xilinx, Inc. admits that the cover of United States Patent No. 7,663,518 (the "'518 Patent") is titled "Dither Technique For Improving Dynamic Non-linearity In An Analog To Digital Converter, And An Analog To Digital Converter Having Improved Dynamic Non-linearity" and states that it was issued on Feb. 16, 2010. Xilinx, Inc. admits that a copy of what appears to be the '518 Patent is attached as Exhibit B to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 13 of the Complaint regarding ownership of the '518 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 13 of the Complaint.

14. Xilinx, Inc. admits that the cover of United States Patent No. 6,900,750 (the "'750 Patent") is titled "Signal Conditioning System With Adjustable Gain And Offset Mismatches" and states that it was issued on May 31, 2005. Xilinx, Inc. admits that a copy of what appears to be the '750 Patent is attached as Exhibit C to the Complaint. Xilinx, Inc. lacks sufficient

information to form a belief regarding the truth of the allegations in Paragraph 14 of the Complaint regarding ownership of the '750 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 14 of the Complaint.

15. Xilinx, Inc. admits that the cover of United States Patent No. 10,250,250 (the "'250 Patent") is titled "Bootstrapped Switching Circuit" and states that it was issued on April 2, 2019. Xilinx, Inc. admits that a copy of what appears to be the '250 Patent is attached as Exhibit D to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 15 of the Complaint regarding ownership of the '250 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 15 of the Complaint.

16. Xilinx, Inc. admits that the cover of United States Patent No. 7,274,321 (the "'321 Patent") is titled "Analog to Digital Converter" and states that it was issued on September 25, 2007. Xilinx, Inc. admits that a copy of what appears to be the '321 Patent is attached as Exhibit E to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 16 of the Complaint regarding ownership of the '321 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 16 of the Complaint.

17. Xilinx, Inc. admits that the cover of United States Patent No. 7,012,463 (the "'463 Patent") is titled "Switched Capacitor Circuit with Reduced Common-Mode Variations" and states that it was issued on March 14, 2006. Xilinx, Inc. admits that a copy of what appears to be the '463 Patent is attached as Exhibit F to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 17 of the

Complaint regarding ownership of the '463 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 17 of the Complaint.

18. Xilinx, Inc. admits that the cover of United States Patent No. 8,487,659 (the "'659 Patent") is titled "Comparator with Adaptive Timing" and states that it was issued on July 16, 2013. Xilinx, Inc. admits that a copy of what appears to be the '659 Patent is attached as Exhibit G to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 18 of the Complaint regarding ownership of the '659 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 18 of the Complaint.

19. Xilinx, Inc. admits that the cover of United States Patent No. 7,286,075 (the "'075 Patent") is titled "Analog to Digital Converter with Dither" and states that it was issued on October 23, 2007. Xilinx, Inc. admits that a copy of what appears to be the '075 Patent is attached as Exhibit H to the Complaint. Xilinx, Inc. lacks sufficient information to form a belief regarding the truth of the allegations in Paragraph 19 of the Complaint regarding ownership of the '075 Patent and therefore denies the allegations. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 19 of the Complaint.

Xilinx's Incorporation of Analog's Patented Technologies into Xilinx's RFSoC Products

20. Xilinx, Inc. denies the allegations contained in Paragraph 20 of the Complaint.

21. Xilinx, Inc. admits that ADI and Xilinx, Inc. previously entered into a non-disclosure agreement. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 21 of the Complaint.

22. Xilinx, Inc. admits that, as of the filing of this Answer, its website at https://www.xilinx.com/products/technology/high-speed-serial/jesd2014-reference-designs.html

states, among other things, that "Xilinx working with our Analog partners provides a rich set of JESD204B reference designs and high-speed analog FMC cards to jump start development," and further states, among other things, "4-chan, 14-bit, 250 MSPS." (Last accessed January 16, 2020.) Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 22 of the Complaint.

23. Xilinx, Inc. admits that, as of the filing of this Answer, its website at https://www.xilinx.com/products/technology/rfsampling.html#overview appears to contain the figure shown in Paragraph 23 of the Complaint. (Last accessed January 16, 2020.) Xilinx, Inc. admits that, as of the filing of this Answer, its website at https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html states, among other things, that the Zynq UltraScale+ RFSoC "[e]liminates discrete converters" and "[r]emoves power hungry FPGA-to-Analog interfaces like JESD204." (Last accessed January 16, 2020.) Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 23 of the Complaint.

24. Xilinx, Inc. denies the allegations contained in Paragraph 24 of the Complaint.

25. Xilinx, Inc. admits that, as of the filing of this Answer, its website at https://www.xilinx.com/products/silicon-devices/soc.html lists, among other things, the "Zynq UltraScale+ RFSoC with RF Data Converters," "Zynq UltraScale+ RFSoC with SD-FEC Cores," and "Zynq UltraScale+ RFSoC with RF Data Converters and SD-FEC Cores" as "High-End." (Last accessed January 11, 2020.) Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 25 of the Complaint.

26. Xilinx, Inc. admits that, as of the filing of this Answer, a copy of the paper *An Adaptable Direct RF-Sampling Solution*, February 20, 2019, is available at Xilinx, Inc.'s website

at https://www.xilinx.com/support/documentation/white_papers/wp489-rfsampling-solutions.pdf. (Last accessed January 16, 2020.) Xilinx, Inc. admits that the Abstract of *An Adaptable Direct RF-Sampling Solution*, February 20, 2019, states, among other things, that "Direct RF-sampling enables a new level adaptability by moving much of the RF signal processing into the digital domain, thereby eliminating much of the analog signal processing[Ref 1][Ref 2]. However, there is immense market pressure to reduce the power and footprint of these systems. The solution is to integrate RF-sampling data converters with VLSI devices using advanced CMOS technology." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 26 of the Complaint.

27. Xilinx, Inc. admits that, as of the filing of this Answer, its website at https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html#documentation contains links to documents relating to Zynq UltraScale+ RFSoC. (Last accessed January 16, 2020.) Xilinx, Inc. admits that, as of the filing of this Answer, a copy of "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, is available at Xilinx, Inc.'s website at https://www.xilinx.com/support/documentation/product-briefs/rfsoc-ieee-paper.pdf. (Last accessed January 16, 2020.) Xilinx, Inc. admits that, as of the filing of this Answer, a copy of "Zynq UltraScale+ RFSoC Data Sheet: Overview" is available at Xilinx, Inc.'s website at https://www.xilinx.com/support/documentation/data_sheets/ds889-zynq-usp-rfsoc-overview.pdf. (Last accessed January 16, 2020.) Xilinx, Inc. admits that a presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," was presented by Xilinx, Inc. at the 2017 IEEE International Solid-State Circuits Conference. Xilinx, Inc. admits that a copy of what appears to be "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits

Digest of Technical Papers, is attached as Exhibit J to the Complaint. Xilinx, Inc. admits that a copy of what appears to be U.S. Patent No. 10,033,395 is attached as Exhibit K to the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 27 of the Complaint.

28. Xilinx, Inc. denies the allegations contained in Paragraph 28 of the Complaint.

COUNT I
(Infringement of U.S. Patent No. 7,719,452)

29. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-28 of the Complaint, as if fully set forth herein.

30. Xilinx, Inc. denies the allegations contained in Paragraph 30 of the Complaint.

31. Xilinx, Inc. admits that an analog-to-digital converter converts an analog signal into a digital signal. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.4 Simplified ADC architecture," and a figure labeled "Fig. 6.7 Simplified ADC channel." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 31 of the Complaint.

32. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.6 Sampling network and clocking." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 32 of the Complaint.

33. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.7 Simplified ADC channel." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 33 of the Complaint.

34. Xilinx, Inc. admits that the paper "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits Digest of Technical Papers, appears to contain the figure shown in Paragraph 34 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 34 of the Complaint.

35. Xilinx, Inc. admits that U.S. Patent No. 10,033,395 appears to contain the figure shown in Paragraph 35 of the Complaint. Xilinx, Inc. admits that the paper "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits Digest of Technical Papers, contains a figure labeled "Fig. 1 ADC architecture." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 35 of the Complaint.

36. Xilinx, Inc. admits that the paper "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits Digest of Technical Papers, appears to contain the figure shown in Paragraph 36 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 36 of the Complaint.

37. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.4 Simplified ADC architecture." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 37 of the Complaint.

38. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '452 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 38 of the Complaint.

39. Xilinx, Inc. denies the allegations contained in Paragraph 39 the Complaint.

40. Xilinx, Inc. denies the allegations contained in Paragraph 40 of the Complaint.

COUNT II
(Infringement of U.S. Patent No. 7,663,518)

41. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-40 of the Complaint, as if fully set forth herein.

42. Xilinx, Inc. denies the allegations contained in Paragraph 42 of the Complaint.

43. Xilinx, Inc. admits that the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, appears to contain the figure shown in Paragraph 43 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 43 of the Complaint.

44. Xilinx, Inc. admits that page 276 of the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, states, among other things: "Each 2GS/S ADC unit consists of four interleaved 500 MS/s sub-ADC slices and a sampling network composed of a front-end switch and four channel switches used to interleave the four ADC slices without time-skew calibration requirements," and "Fig. 16.1.1b shows the topology of each sub-ADC. It uses three asynchronous 5b SAR stages separated by two residue amplifiers (RA). For speed reasons, each stage uses a split-capacitor MDAC to maintain constant common mode and five cascaded dynamic comparators." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 44 of the Complaint.

45. Xilinx, Inc. admits that slide 21 of the presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at the 2017 IEEE International Solid-State Circuits Conference, appears to contain the figure shown in Paragraph

45 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 45 of the Complaint.

46. Xilinx, Inc. admits that the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, appears to contain the figure shown in Paragraph 46 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 46 of the Complaint.

47. Xilinx, Inc. admits that slide 20 of the presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at the 2017 IEEE International Solid-State Circuits Conference, appears to contain the figure shown in Paragraph 47 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 47 of the Complaint.

48. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '518 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 48 of the Complaint.

49. Xilinx, Inc. denies the allegations contained in Paragraph 49 of the Complaint.

50. Xilinx, Inc. denies the allegations contained in Paragraph 50 of the Complaint.

COUNT III
(Infringement of U.S. Patent No. 6,900,750)

51. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-50 of the Complaint, as if fully set forth herein.

52. Xilinx, Inc. denies the allegations contained in Paragraph 52 of the Complaint.

53. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.4 Simplified ADC architecture," and a figure labeled "Fig. 6.7 Simplified ADC channel."

Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 53 of the Complaint.

54. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.4 Simplified ADC architecture." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 54 of the Complaint

55. Xilinx, Inc. admits that the paper "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits Digest of Technical Papers, appears to contain the figure shown in Paragraph 55 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 55 of the Complaint.

56. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.9 Offset sources in ADC and impact of where offset calibration is done." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 56 of the Complaint.

57. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '750 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 57 of the Complaint.

58. Xilinx, Inc. denies the allegations contained in Paragraph 58 of the Complaint.

59. Xilinx, Inc. denies the allegations contained in Paragraph 59 of the Complaint.

COUNT IV
(Infringement of U.S. Patent No. 10,250,250)

60. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-59 of the Complaint, as if fully set forth herein.

61. Xilinx, Inc. denies the allegations contained in Paragraph 61 of the Complaint.

62. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.6 Sampling network and clocking." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 62 of the Complaint.

63. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.6 Sampling network and clocking." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 63 of the Complaint.

64. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.6 Sampling network and clocking." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 64 of the Complaint.

65. Xilinx, Inc. denies the allegations contained in Paragraph 65 of the Complaint.

66. Xilinx, Inc. denies the allegations contained in Paragraph 66 of the Complaint.

67. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '250 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 67 of the Complaint.

68. Xilinx, Inc. denies the allegations contained in Paragraph 68 of the Complaint.

69. Xilinx, Inc. denies the allegations contained in Paragraph 69 of the Complaint.

COUNT V
(Infringement of U.S. Patent No. 7,274,321)

70. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-69 of the Complaint, as if fully set forth herein.

71. Xilinx, Inc. denies the allegations contained in Paragraph 71 of the Complaint.

72. Xilinx, Inc. admits that the Accused RFSoC Products include multiple analog-to-digital converters. Xilinx, Inc. admits that, as of the filing of this Answer, the "Zynq UltraScale+ RFSoC Data Sheet: Overview," available at https://www.xilinx.com/support/documentation/data_sheets/ds889-zynq-usp-rfsoc-overview.pdf (last accessed January 16, 2020), appears to contain the figure shown in Paragraph 72 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 72 of the Complaint.

73. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.7 Simplified ADC channel." Xilinx, Inc. admits that Slide 11 of the presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at the 2017 IEEE International Solid-State Circuits Conference, appears to contain the second figure shown in Paragraph 73 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 73 of the Complaint.

74. Xilinx, Inc. admits that page 276 of the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, states, among other things: "Each 2GS/S ADC unit consists of four interleaved 500 MS/s sub-ADC slices and a sampling network composed of a front-end switch and four channel switches used to interleave

the four ADC slices without time-skew calibration requirements." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 74 of the Complaint.

75. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.7 Simplified ADC channel." Xilinx, Inc. admits that slide 15 of the presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at the 2017 IEEE International Solid-State Circuits Conference, appears to contain the figure shown in Paragraph 75 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 75 of the Complaint.

76. Xilinx, Inc. denies the allegations contained in Paragraph 76 of the Complaint.

77. Xilinx, Inc. admits that the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, appears to contain the figure shown in Paragraph 77 of the Complaint. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.7 Simplified ADC channel." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 77 of the Complaint.

78. Xilinx, Inc. admits that the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, appears to contain the figure shown in Paragraph 78 of the Complaint. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.7 Simplified ADC channel." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 78 of the Complaint.

79. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '321 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 79 of the Complaint.

80. Xilinx, Inc. denies the allegations contained in Paragraph 80 of the Complaint.

81. Xilinx, Inc. denies the allegations contained in Paragraph 81 of the Complaint.

COUNT VI
(Infringement of U.S. Patent No. 7,012,463)

82. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-81 of the Complaint, as if fully set forth herein.

83. Xilinx, Inc. denies the allegations contained in Paragraph 83 of the Complaint.

84. Xilinx, Inc. admits that the Accused RFSoC Products are integrated circuits. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 84 of the Complaint.

85. Xilinx, Inc. admits that slide 23 of the presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at the 2017 IEEE International Solid-State Circuits Conference, appears to contain the figure shown in Paragraph 85 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 85 of the Complaint.

86. Xilinx, Inc. denies the allegations contained in Paragraph 86 of the Complaint.

87. Xilinx, Inc. denies the allegations contained in Paragraph 87 of the Complaint.

88. Xilinx, Inc. denies the allegations contained in Paragraph 88 of the Complaint.

89. Xilinx, Inc. denies the allegations contained in Paragraph 89 of the Complaint.

90. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '463 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 90 of the Complaint.

91. Xilinx, Inc. denies the allegations contained in Paragraph 91 of the Complaint.

92. Xilinx, Inc. denies the allegations contained in Paragraph 92 of the Complaint.

COUNT VII
(Infringement of U.S. Patent No. 8,487,659)

93. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-92 of the Complaint, as if fully set forth herein.

94. Xilinx, Inc. denies the allegations contained in Paragraph 94 of the Complaint.

95. Xilinx, Inc. denies the allegations contained in Paragraph 95 of the Complaint.

96. Xilinx, Inc. admits that slide 24 of the presentation titled "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC," presented at the 2017 IEEE International Solid-State Circuits Conference, appears to contain the figure shown in Paragraph 96 of the Complaint. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 96 of the Complaint.

97. Xilinx, Inc. denies the allegations contained in Paragraph 97 of the Complaint.

98. Xilinx, Inc. admits that the Accused RFSoC Products are integrated circuits. Xilinx, Inc. admits that page 276 of the paper "A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC", Vaz et al., February 2017, states, among other things: "A single RA design is used to reduce design/verification effort, with only a minor penalty to power consumption. The gain of the integrating RA is adjusted by appropriately sizing its load capacitance. The FG calibration corrects comparator offsets, RA offset and gain and capacitor mismatch. The BG calibration adjusts the RA gain and comparator offset drift due to temperature

and voltage variations during operation. … Figure 16.1.2a details the clock interface of the pipelined-SAR ADC. The integration time of the RAs varies considerably across PVT, and leakage limits the achievable performance of the ADC at low sampling frequencies if using a synchronous clocking scheme." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 98 of the Complaint.

99. Xilinx, Inc. admits that on July 31, 2019, ADI provided Xilinx, Inc. with a claim chart for the '659 Patent. Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 99 of the Complaint.

100. Xilinx, Inc. denies the allegations contained in Paragraph 100 of the Complaint.

101. Xilinx, Inc. denies the allegations contained in Paragraph 101 of the Complaint.

COUNT VIII
(Infringement of U.S. Patent No. 7,286,075)

102. Xilinx, Inc. repeats and incorporates by reference its responses to Paragraphs 1-101 of the Complaint, as if fully set forth herein.

103. Xilinx, Inc. denies the allegations contained in Paragraph 103 of the Complaint.

104. Xilinx, Inc. admits that an analog-to-digital converter converts an analog signal into a digital signal. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.4 Simplified ADC architecture," and a figure labeled "Fig. 6.7 Simplified ADC channel." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 104 of the Complaint.

105. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled

"Fig. 6.7 Simplified ADC channel." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 105 of the Complaint.

106. Xilinx, Inc. admits that the paper "A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET," Vaz, et al., 2018 VLSI Symposium on VLSI Circuits Digest of Technical Papers, appears to contain the figure shown in Paragraph 106 of the Complaint. Xilinx, Inc. admits that the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, contains a figure labeled "Fig. 6.7 Simplified ADC channel." Xilinx, Inc. admits that page 98 of the paper titled "High-speed ADCs for Wireless Base-Stations," by Verbruggen et al., attached as Exhibit I to the Complaint, states, among other things: "These errors are randomized by injecting a 3.7b PRBS dither signal just after sampling." Except as expressly admitted, Xilinx, Inc. denies the remaining allegations of Paragraph 106 of the Complaint.

107. Xilinx, Inc. denies the allegations contained in Paragraph 107 of the Complaint.

108. Xilinx, Inc. denies the allegations contained in Paragraph 108 of the Complaint.

109. Xilinx, Inc. denies the allegations contained in Paragraph 109 of the Complaint.

REQUEST FOR RELIEF

Xilinx, Inc. denies that ADI is entitled to any relief in this action and asks the Court to deny any and all of the relief requested by ADI in its Complaint. Further, and to the extent that the Complaint's Prayer for Relief includes any factual allegations, Xilinx, Inc. denies those allegations.

JURY DEMAND

Allegations regarding a jury demand are legal matters that do not require a response.

ADDITIONAL DEFENSES

Xilinx, Inc. hereby asserts the following separate additional defenses to the claims and allegations in ADI's Complaint, without admitting or acknowledging that Xilinx, Inc. bears the burden of proof as to any of them.

FIRST ADDITIONAL DEFENSE

(Non-Infringement)

110. Xilinx, Inc. does not infringe and has not infringed valid and enforceable claims of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents, whether directly or indirectly, by inducement or contributory infringement, literally, or under the doctrine of equivalents.

SECOND ADDITIONAL DEFENSE

(Invalidity)

111. One or more claims of each of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents is invalid for failure to comply with one or more requirements for patentability, including, but not limited to, those set forth in one or more of 35 U.S.C. §§ 101, 102, 103, and/or 112.

THIRD ADDITIONAL DEFENSE

(Estoppel)

112. One or more of ADI's claims is barred, in whole or in part, by the doctrine of estoppel, including, but not limited to, prosecution history estoppel arising from a patentee's actions, representations, or conduct before the United States Patent and Trademark Office during the prosecutions of each of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents, and equitable estoppel and estoppel by acquiescence arising from ADI's actions and inactions.

FOURTH ADDITIONAL DEFENSE

(Limitations on Damages)

113. To the extent ADI seeks recovery for any alleged infringement committed prior to the filing of the Complaint, such recovery is barred in whole or in part by 35 U.S.C. §§ 286 and/or 287.

FIFTH ADDITIONAL DEFENSE

(Limitation on Recovery of Costs)

114. ADI is precluded from seeking recovery of costs by 35 U.S.C. § 288.

SIXTH ADDITIONAL DEFENSE

(Failure to State a Claim)

115. ADI's claims for alleged infringement of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents fail to state a claim upon which relief can be granted.

SEVENTH ADDITIONAL DEFENSE

(Government Sales)

116. ADI is precluded from obtaining any remedy against Xilinx, Inc. for products used by or manufactured for the United States under 28 U.S.C. § 1498(a).

EIGHTH ADDITIONAL DEFENSE

(No Willful Infringement)

117. Xilinx, Inc. has not willfully infringed, and is not willfully infringing, valid and enforceable claims of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents. ADI is not entitled to seek enhanced damages or attorneys' fees for any such alleged willful infringement.

NINTH ADDITIONAL DEFENSE

(License and Exhaustion)

118. ADI's claims for patent infringement are precluded in whole or in part (i) to the extent that any allegedly infringing Xilinx, Inc. products or components thereof are or were imported, sold by, offered for sale by, made by, or made for, any entity or entities having express or implied licenses to the '452, '518, '750, '250, '321, '463, '659, and/or '075 Patents and/or (ii) under the doctrine of patent exhaustion.

RESERVATION OF RIGHTS

119. Xilinx, Inc. reserves the right to amend its Answer as of right or to otherwise seek leave to amend its Answer to plead additional defenses and counterclaims and/or to supplement its existing defenses if information developed through discovery, trial, or otherwise merits such additional defenses, counterclaims, and/or supplementation.

COUNTERCLAIMS

Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively, "Xilinx") bring the following Counterclaims against Plaintiff Analog Devices, Inc. ("ADI"):

NATURE OF THE COUNTERCLAIMS

1. Xilinx is a pioneering semiconductor chip designer based in San Jose, California. It was founded in 1984 by Ross Freeman, Bernard Vonderschmitt, and James V. Barnett II. Xilinx leads the semiconductor industry in the field of adaptive and intelligent computing.

2. Xilinx is the established market leader in programmable logic devices ("PLDs"). PLDs are integrated circuits in which the functions of the internal logical gates are programmable instead of fixed. Accordingly, end users can customize the PLDs for use in specific applications. Xilinx customers use its PLDs in wide-ranging applications, such as wireless communications, cloud computing, video processing, and automobiles.

3. Xilinx's commercial success is rooted in its history of innovation. For example, one of the co-founders of Xilinx, Ross Freeman, invented the field programmable gate array ("FPGA"), a novel PLD structure that reshaped the semiconductor industry and for which Xilinx is renowned. An FPGA comprises "open gates" that engineers can reprogram as needed to add new functionality, adapt to changing standards or specifications, and make last minute design changes.

4. For his contributions to the semiconductor industry, Mr. Freeman was inducted to the National Inventors Hall of Fame in 2009. Other notable inductees to the National Inventors Hall of Fame include Thomas Edison, Alexander Graham Bell, and Steve Jobs.

5. Xilinx continues to disrupt the industry through technology breakthroughs such as the adaptive compute acceleration platform ("ACAP"), a new type of PLD that goes far beyond the capabilities of an FPGA. ACAP is a revolutionary new heterogeneous compute architecture

that delivers world-class vector and scalar processing elements tightly coupled to next-generation programmable logic, all tied together with a high-bandwidth network-on-chip, which provides memory-mapped access to all three types of architectures (*i.e.*, scalar processing elements, vector processing elements, and programmable logic). ACAP-based products can be changed at both hardware and software levels to dynamically adapt to the needs of a broad set of applications in the emerging era of big data and artificial intelligence, including video transcoding, database, data compression, search, AI interference, genomics, machine vision, computational storage, and network acceleration.

6. Xilinx's ongoing innovation leadership is recognized throughout the semiconductor industry. For example, in 2018, Xilinx's CEO, Victor Peng, was named Innovator of the Year at the 2018 World Electronic Achievement Awards. And in 2019, MIT Technology Review named Xilinx as one of its 50 Smartest Companies.

7. The United States Patent and Trademark Office ("PTO") has granted over 4,000 patents for Xilinx's inventions. The patents that Xilinx asserts in this lawsuit protect several groundbreaking inventions with important applications in modern integrated circuits.

8. Xilinx has made important advances in RF signal chain technologies and has been awarded a significant number of patents by the PTO for these important innovations. ADI has wrongfully coopted Xilinx's patented technologies by incorporating them into ADI's products without Xilinx's authorization. The infringing ADI products include, for example, high speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), wideband RF transceivers with configurable SerDes interfaces, and mixed-signal front-end devices.

9. Xilinx brings these Counterclaims to put an end to ADI's infringement of Xilinx's patents.

XILINX ASSERTED PATENTS AND ACCUSED ADI PRODUCTS

10. These Counterclaims arise under the patent laws of the United States, codified at 35 U.S.C. §§ 1, *et seq.*, over which this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 (federal question) and 1338(a) (action arising under an Act of Congress relating to patents) for infringement of: U.S. Patent Nos. 6,975,132 (the "'132 patent"), attached hereto as Exhibit 1; 7,015,838 (the "'838 patent"), attached hereto as Exhibit 2; 7,088,767 (the "'767 patent"), attached hereto as Exhibit 3; 7,116,251 (the "'251 patent"), attached hereto as Exhibit 4; 7,187,709 (the "'709 patent"), attached hereto as Exhibit 5; 7,224,184 (the "'184 patent"), attached hereto as Exhibit 6; 7,280,590 (the "'590 patent"), attached hereto as Exhibit 7; and 8,548,071 (the "'071 patent"), attached hereto as Exhibit 8, (collectively, the "Xilinx Patents"). Xilinx has not licensed any of the Xilinx Patents to ADI.

11. This action arises out of the manufacture, use, importation, offer for sale, and/or sale by ADI of products that practice one of more claims of the Xilinx Patents (collectively, "Accused Products"). By way of example, and without limitation, the Accused Products include:

- AD9213, AD9208, AD9081/2, AS9697, AD9689, AD9695, AD6688, ADN4612, and ADN8102, all versions or variations of the foregoing devices including evaluation and reference design products, and any other devices comprising a digital emphasis circuit in a current-driven transmitter circuit, as recited in or otherwise equivalent to one or more claims of the '132 patent, made, used, sold, offered for sale, or imported since the issuance of the '132 patent (collectively, "'132 Infringing Products");

- AD6688, AD9208, AD9213, AD9625, AD9689, AD9144, AD9152, AD9161, AD9162, AD9163, AD9164, AD9171, AD9172, AD9173, AD9174, AD9175, AD9176, ADRV9008-1, ADRV9008-2, ADRV9009, and ADRV9026, all versions or variations of the foregoing devices including evaluation and reference design products, and any other ADI products that include a programmable serial data path, as recited in or otherwise equivalent to one or more claims of the ’838 patent, made, used, sold, offered for sale, or imported since the issuance of the ’838 patent (collectively, “’838 Infringing Products”);
- AD9081 and AD9082, all versions or variations of the foregoing devices including evaluation and reference design products, and any other devices that includes a transceiver for sending and receiving data at a lower data rate than the designed serializing data rate, as recited in or otherwise equivalent to one or more claims of the ’767 patent, made, used, sold, offered for sale, or imported since the issuance of the ’767 patent (collectively,“’767 Infringing Products”);
- AD6688, AD9208, AD9213, AD9625, AD9689, AD9144, AD9152, AD9161, AD9162, AD9163, AD9164, AD9171, AD9172, AD9173, AD9174, AD9175, AD9176, ADRV9008-1, ADRV9008-2, ADRV9009, and ADRV9026, all versions or variations of the foregoing devices including evaluation and reference design products, and any other ADI products that include a programmable serial data path, as recited in or otherwise equivalent to one or more claims of the ’251 patent, made, used, sold, offered for sale, or imported since the issuance of the ’251 patent (collectively, “’251 Infringing Products”);

- ADRV9008-1, ADRV9008-2, ADRV9009, ADRV9026, AD9371, AD9375, AD9081, and AD9082, all versions or variations of the foregoing products including evaluation and reference design products, and any other ADI products that include a configurable transceiver with a loss of synchronization detector, as recited in or otherwise equivalent to one or more claims of the '709 patent, made, used, sold, offered for sale, or imported since the issuance of the '709 patent (collectively, "'709 Infringing Products");
- AD9208, AD9176, AD6674, AD6679, AD6684, AD6688, AD9656, AD9680, AD9684, AD9689, AD9690, AD9691, AD9694, AD9695, AD9697, AD9234, AD9081, and AD9082, all versions or variations of the foregoing devices including evaluation and reference design products, and any other ADI products that include reconfigurable crossbar mux, as recited in or otherwise equivalent to one or more claims of the '184 patent made, used, sold, offered for sale, or imported since the issuance of the '184 patent (collectively, "'184 Infringing Products");
- AD9161, AD9162, AD9163, AD9164, AD9171, AD9172, AD9173, AD9174, AD9175, and AD9176, all versions or variations of the foregoing devices including evaluation and reference design products, and any other ADI products that include a receiver terminal network with an analog front-end and a data recovery module, as recited in or otherwise equivalent to one or more claims of the '590 patent, made, used, sold, offered for sale, or imported since the issuance of the '590 patent (collectively, "'590 Infringing Products"); and

- AD9625, AD9652, and AD9680, all versions or variations of the foregoing devices including evaluation and reference design products, and any other devices comprising at least two time-interleaved analog-to-digital converters integrated onto a single circuit, as recited in or otherwise equivalent to one or more claims of the '071 patent, made, used, sold, offered for sale, or imported since the issuance of the '071 patent (collectively, "'071 Infringing Products").

JURISDICTION AND VENUE

12. Xilinx, Inc. is a corporation incorporated under the laws of the State of Delaware. Its principal place of business is at 2100 Logic Drive, San Jose, California 95124.

13. Xilinx Asia Pacific Pte. Ltd. is a private limited corporation organized under the laws of Singapore. Its principal place of business is at 5 Changi Business Park Vista, Singapore 486 040.

14. Upon information and belief, ADI is a Massachusetts corporation with its corporate headquarters located at One Technology Way, Norwood, Massachusetts 02062.

15. These Counterclaims arise under federal statutory law, including 35 U.S.C. § 271 *et seq*. Accordingly, this Court has subject matter jurisdiction over these Counterclaims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

16. To the extent that venue is found to be proper under 28 U.S.C. § 1400 for any of the claims in the Complaint, venue is also appropriate under 28 U.S.C. § 1400 for these Counterclaims. Venue and jurisdiction are proper within this District because, *inter alia*, ADI has sought the benefit of this forum for this litigation.

FIRST COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 6,975,132

17. Xilinx realleges and incorporates by reference paragraphs 1-16 of these Counterclaims as if fully set forth herein.

18. The '132 patent was duly and legally issued by the PTO on December 13, 2005, and is titled "DAC Based Driver with Selectable Pre-Emphasis Signal Levels."

19. Xilinx possesses all ownership rights, title, and interests in the '132 patent.

20. ADI has infringed, currently infringes, and will continue to infringe at least claim 19 of the '132 patent. ADN4612 is representative of infringement by the '132 Infringing Products.

21. Claim 19 of the '132 patent states:

A method in a Tx line driver for generating a pre-emphasis signal for a first bit following a transition in a data stream, comprising:

transmitting pre-emphasis current setting signals to a first current selection module to prompt the current selection module to generate a specified amount of reference current upon receiving a pre-emphasis signal;

determining whether a transition has occurred in the data bit stream from one bit to another;

producing the pre-emphasis control signal;

producing the pre-emphasis current; and

summing the pre-emphasis current and a primary current in an outgoing data stream.

22. ADN4612 meets all limitations of claim 19 of the '132 patent.

23. ADI's data sheet for ADN4612 is attached as Exhibit 9. Excerpts from pages 1 and 27 of the data sheet are reproduced below.

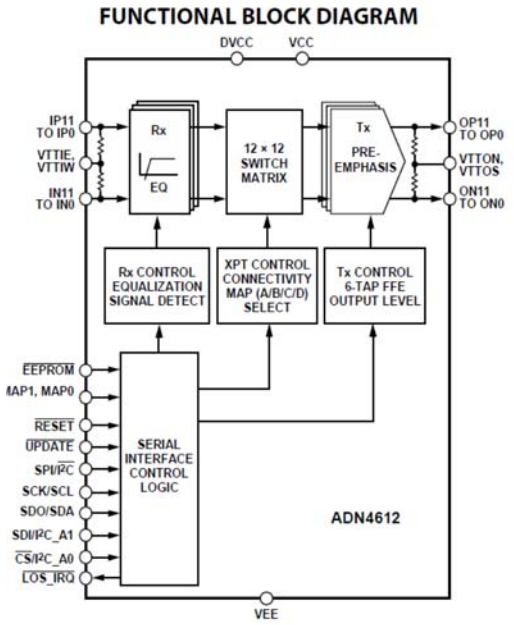


Figure 1.

(Exhibit 9 at 1.)

TRANSMITTERS

Output Structure

The ADN4612 transmitter outputs incorporate 50 Ω termination resistors, ESD protection, and a CML style driver with a programmable tail current (see Figure 55). Each channel includes a fully programmable, six-tap FFE. The flexible programmability of the FFE enables a broad range of output filter shapes to compensate for signal impairments, such as intersymbol interference (ISI), caused by channel attenuation.

(*Id.* at 27.)

Multitap Feedforward Equalizer

A block diagram of the FFE is shown in Figure 54. The FFE consists of eight output current driver elements (PC and D0 to D6) with a maximum of 16 mA per driver and five delay line elements (τ) arranged to create a six-tap FFE with individually programmable coefficients. A summing junction at the output combines the output currents of all the drivers into the load.

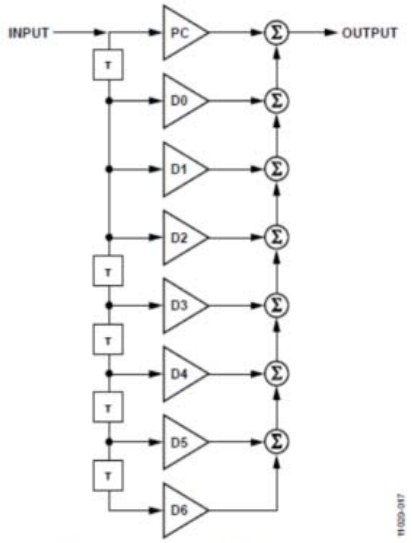


Figure 54. Output FFE Block Diagram

The main tap comprises three independent output driver elements (D0, D1, and D2). The precursor tap (PC) and the four postcursor taps (D3, D4, D5, and D6) are each individual output drivers. The tap delay, τ, is optimized for 11.3 Gbps data rates. This flexible implementation enables both preemphasis and deemphasis. The FFE architecture also facilitates shifting the location of the main tap to create multiple precursors.

Each driver is controlled by a 4-bit output level value and sign code, a 2-bit resolution value, and a 2-bit enable. The output current per tap (in mA) is listed in Table 15 for the corresponding output level and resolution codes. The MSB of the output level is the sign bit and the three LSBs represent a 3-bit magnitude. To convert the table from mA to mV p-p differential, use the following equation:

$$V_{Dx} = (2 \times I_{Dx}) \times (50\ \Omega || 50\ \Omega)$$

Table 15. Driver Element Current (mA) and Resolution Codes

Driver Current Level Codes (Binary)	Resolution Codes			
	00b (Full Scale)	01b (Half Scale)	10b (Quarter Scale)	11b (Eighth Scale)
0000	+2	+1	+0.5	+0.25
0001	+4	+2	+1.0	+0.5
0010	+6	+3	+1.5	+0.75
0011	+8	+4	+2.0	+1.0
0100	+10	+5	+2.5	+1.25
0101	+12	+6	+3.0	+1.5
0110	+14	+7	+3.5	+1.75
0111	+16	+8	+4.0	+2.0
1000	−2	−1	−0.5	−0.25
1001	−4	−2	−1.0	−0.5
1010	−6	−3	−1.5	−0.75
1011	−8	−4	−2.0	−1.0
1100	−10	−5	−2.5	−1.25
1101	−12	−6	−3.0	−1.5
1110	−14	−7	−3.5	−1.75
1111	−16	−8	−4.0	−2.0

(*Id.* at 27.)

24. ADN4612 performs a method in a Tx line driver for generating a pre-emphasis signal for a first bit following a transition in a data stream. The Tx line driver includes the pre-emphasis current driver and current selection module discussed below.

25. The ADN4612 is current driven. For example, page 27 of the data sheet states that the output structure of the ADN4612 incorporates a "CML style driver." (Exhibit 9 at 27.) CML means "current-mode logic."

26. The Tx line driver in the ADN4612 transmits pre-emphasis current setting signals to a first current selection module to prompt the current selection module to generate a specified amount of reference current upon receiving a pre-emphasis signal. For example, Figure 1 of the

data sheet shows that the Tx line driver contains a module designated "Tx PRE-EMPHASIS." (Exhibit 9 at 1.) Details of the pre-emphasis current driver are shown in Figure 54 of the data sheet (reproduced above). For example, Figure 54 shows that the pre-emphasis module comprises a multitap feedforward equalizer ("FFE"). (*Id.* at 27.) Page 27 of the data sheet say that each tap of the FFE is programmable. Furthermore, Figure 54 of the data sheet shows that the FFE in the ADN4612 contains several taps that are delayed from each other by "delay line elements." (*Id*.) These taps, together with the gain elements D0–D6, act to adjust the amount of pre-emphasis current in response to transitions in the outgoing data stream.

27. The ADN4612 determines whether a transition has occurred in the data bit stream from one bit to another. For example, the taps and gain elements determine whether said transitions have occurred.

28. The ADN4612 produces a pre-emphasis control signal. For example, Page 1 of the data sheet shows that the ADN4612 contains a Tx Control module that provides a pre-emphasis control signal to the TX Pre-Emphasis module.

29. The ADN4612 produces a pre-emphasis current. For example, Page 1 of the data sheet shows that the ADN4612 contains a Tx Pre-Emphasis Module that produces the pre-emphasis current. Moreover, Figure 43 of the data sheet shows that the delayed gain elements produce a pre-emphasis current.

30. The ADN4612 sums the pre-emphasis current and a primary current in an outgoing data stream. For example, Figure 43 of the data sheet shows that the pre-emphasis current generated by the delayed gain elements is summed with the primary current.

31. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '132 patent, including at least claim 19, literally or under the doctrine of

equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing in the United States the '132 Infringing Products. For example, ADI performs the method of claim 19 when it uses the '132 Infringing Products for testing purposes.

32. At least as of the filing of this Counterclaim, ADI has knowledge of the '132 patent.

33. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '132 patent, including at least claim 19, under 35 U.S.C. § 271(b) by customers and other end users of the '132 Infringing Products in the United States. ADI's acts of inducement include at least selling the '132 Infringing Products, which are configured to infringe the '132 patent. These acts actively encourage and induce customers and other end users of the '132 Infringing Products to directly infringe at least claim 19 of the '132 patent by using the products in the United States.

34. ADI is committing these acts of infringement of the '132 patent without license or authorization.

35. As a result of ADI's infringement of the '132 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

36. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '132 Infringing Products infringe the '132 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '132 patent.

37. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

SECOND COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 7,015,838

38. Xilinx repeats and incorporates by reference paragraphs 1-37 of these Counterclaims as if fully set forth herein.

39. The '838 patent was duly and legally issued by the PTO on March 21, 2006, and is titled "Programmable Serializing Data Path."

40. Xilinx possesses all ownership rights, title, and interests in the '838 patent.

41. ADI has infringed, currently infringes, and will continue to infringe at least claim 1 of the '838 patent. AD9208 is representative of infringement by the '838 Infringing Products.

42. Claim 1 of the '838 patent states:

> A programmable serializing data path comprises:
>
> programmable timing circuit operably coupled to generate a first plurality of timing signals when the width of parallel input data is of a first multiple and to generate a second plurality of timing signals when the width of the parallel input data is of a second multiple; and
>
> parallel to serial module operably coupled to convert the parallel input data into serial output data based on the first or second plurality of timing signals.

43. Excerpts from the AD9208 data sheet, attached as Exhibit 10, are reproduced below:

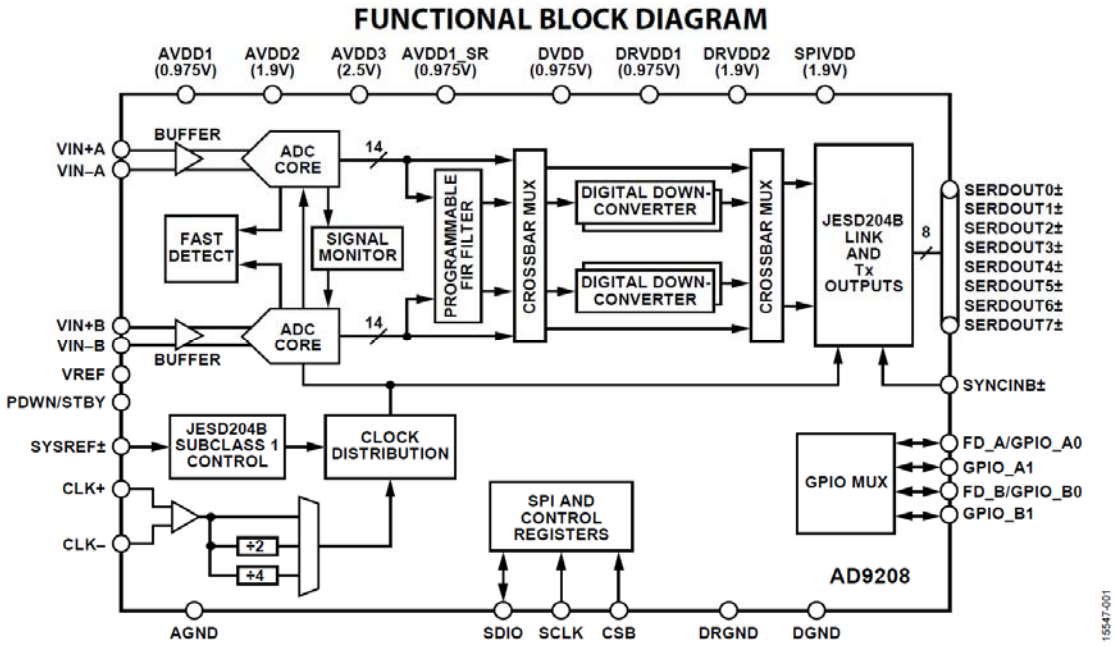


Figure 1.

(Exhibit 10 at 1.)

The AD9208 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, four, or eight JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9208 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link); AD9208 value = 1, 2, 4, or 8.
- M is the number of converters per converter device (virtual converters per link); AD9208 value = 1, 2, 4, or 8.
- F is the octets per frame; AD9208 value = 1, 2, 4, 8, or 16.
- N′ is the number of bits per sample (JESD204B word size); AD9208 value = 8 or 16.
- N is the converter resolution; AD9208 value = 7 to 16.
- CS is the number of control bits per sample; AD9208 value = 0, 1, 2, or 3.

(*Id.* at 67.)

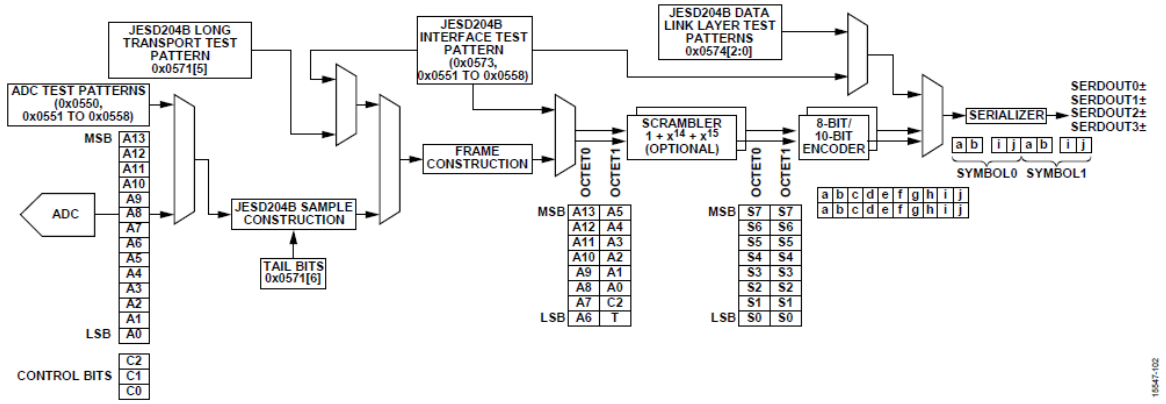


Figure 107. ADC Output Datapath Showing Data Framing

(*Id.* at 68.)

The maximum lane rate allowed by the AD9208 is 16 Gbps. The lane rate is related to the JESD204B parameters using the following equation:

$$Lane\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where $f_{OUT} = \frac{f_{ADC_CLOCK}}{Decimation\ Ratio}$

(*Id.* at 72.)

The AD9208 has one JESD204B link. The serial outputs (SERDOUT0± to SERDOUT7±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

(*Id.*)

0x058E	JESD204B link number of converters (M)	[7:0]	JESD204B M configuration		JESD204B number of converters per link/device (M = JESD204B M configuration).	0x1	R/W
				0	Link connected to one virtual converter (M = 1).		
				1	Link connected to two virtual converters (M = 2).		
				11	Link connected to four virtual converters (M = 4).		
				111	Link connected to eight virtual converters (M = 8).		
0x058F	JESD204B number of control bits (CS) and ADC resolution (N)	[7:6]	Number of control bits (CS) per sample			0x0	R/W
				0	No control bits (CS = 0).		
				1	1 control bit (CS = 1), Control Bit 2 only.		
				10	2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only.		
				11	3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).		
		5	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)			0xF	R/W
				00110	N = 7-bit resolution.		
				00111	N = 8-bit resolution.		
				01000	N = 9-bit resolution.		
				01001	N = 10-bit resolution.		
				01010	N = 11-bit resolution.		
				01011	N = 12-bit resolution.		
				01100	N = 13-bit resolution.		
				01101	N = 14-bit resolution.		
				01110	N = 15-bit resolution.		
				01111	N = 16-bit resolution.		

(*Id.* at 117.)

Phase-Locked Loop (PLL)

The PLL generates the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL locked status bit (Register 0x056F, Bit 7). This read only bit notifies the user if the PLL achieved a lock for the specific setup. Register 0x056F also has a loss of lock (LOL) sticky bit (Bit 3) that notifies the user that a loss of lock is detected. The sticky bit can be reset by issuing a JESD204B link restart (Register 0x0571 = 0x15, followed by Register 0x0571 = 0x14). Refer to Table 32 for the reinitialization of the link following a link power cycle.

The JESD204B lane rate control, Bits[7:4] of Register 0x056E, must be set to correspond with the lane rate. Table 31 shows the lane rates supported by the AD9208 using Register 0x056E.

Table 31. AD9208 Register 0x056E Supported Lane Rates

Value	Lane Rate
0x00	Lane rate = 6.75 Gbps to 13.5 Gbps
0x10	Lane rate = 3.375 Gbps to 6.75 Gbps
0x30	Lane rate = 13.5 Gbps to 15.5 Gbps (default for AD9208)
0x50	Lane rate = 1.6875 Gbps to 3.375 Gbps

(*Id.* at 70.)

44. The AD9208 includes a programmable serializing data path, as discussed below.

45. The AD9208 includes a programmable timing circuit operably coupled to generate a first plurality of timing signals when the width of parallel input data is of a first

multiple and to generate a second plurality of timing signals when the width of the parallel input data is of a second multiple. For example, the AD9208 includes a phase-locked loop that generates a serializer clock in accordance with lane rate control (set in register 0x056E). The lane rate is in turn dependent upon the number of converters ("M") per link (as shown by the lane rate equation reproduced above). (Exhibit 10 at 72.) Different "M" values correspond to the number of converters used and different widths of the parallel data for input into the serializer.

46. The AD9208 also includes a parallel-to-serial module operably coupled to convert the parallel input data into serial output data based on the first or second plurality of timing signals. For example, the JESD204B link, shown in Figure 1 (reproduced above) converts parallel data into serial data based on a timing signal generated by the phase-locked loop discussed above.

47. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '838 patent, including at least claim 1, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing in the United States the '838 Infringing Products.

48. At least as of the filing of this Counterclaim, ADI has knowledge of the '838 patent.

49. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '838 patent, including at least claim 1, under 35 U.S.C. § 271(b) by customers and other end users of the '838 Infringing Products in the United States. ADI's acts of inducement include at least selling the '838 Infringing Products.

These acts actively encourage and instruct customers and other end users of the '838 Infringing Products to directly infringe in the United States at least claim 1 of the '838 patent.

50. ADI is committing these acts of infringement of the '838 patent without license or authorization.

51. As a result of ADI's infringement of the '838 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

52. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '838 Infringing Products infringe the '838 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '838 patent.

53. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

THIRD COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 7,088,767

54. Xilinx repeats and incorporates by reference paragraphs 1-53 of these Counterclaims as if fully set forth herein.

55. The '767 patent was duly and legally issued by the PTO on August 8, 2006, and is titled "Method and Apparatus for Operating A Transceiver in Different Data Rates."

56. Xilinx possesses all ownership rights, title, and interests in the '767 patent.

57. ADI has infringed, currently infringes, and will continue to infringe at least claim 1 of the '767 patent. AD9082 is representative of infringement by the '767 Infringing Products.

58. Claim 1 of the '767 patent states:

A transceiver connected to a data source and a data receiver, comprising:

an input port for accepting a control signal having a first and a second state;

a serializer designed to operate at a first data rate; and

a first interface that receives a first set of data from the data source at a second data rate and delivers a second set of data to the serializer at the first data rate, the second data rate being lower than the first data rate when the control signal is at the first state and the second rate being same as the first data rate when the control signal is at the second state.

59. Excerpts from the AD9082 data sheet, attached as Exhibit 11, are reproduced below:

FUNCTIONAL BLOCK DIAGRAM

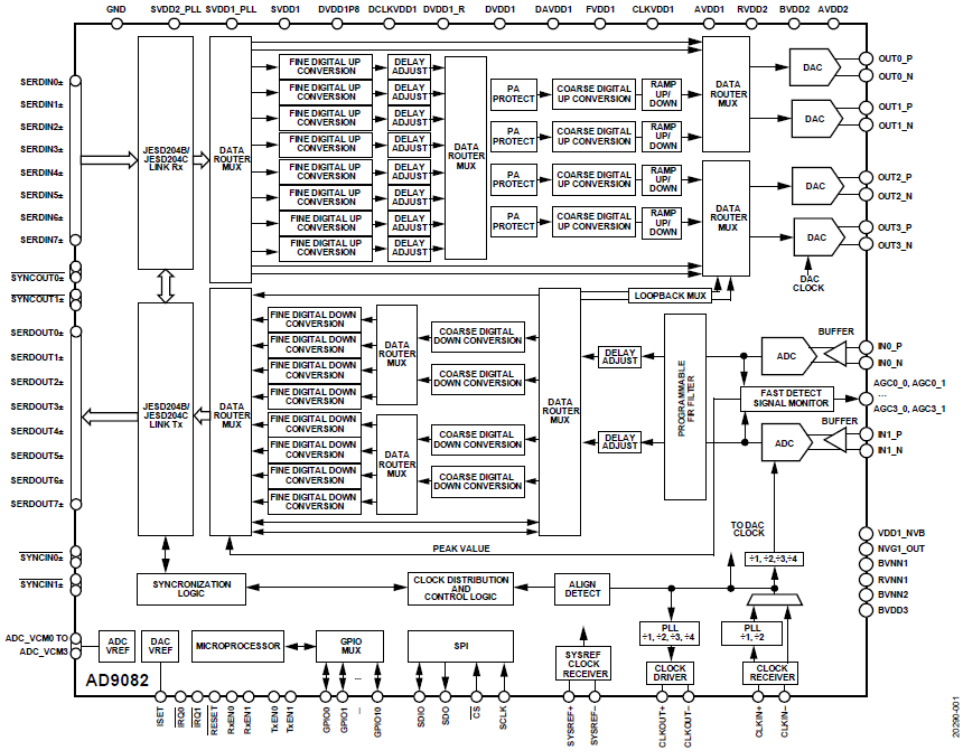


Figure 1. Functional Block Diagram

(Exhibit 11 at 2.)

SERDES JESD204B/JESD204C interface, 16 lanes up to 24.75 Gbps
- **8 receive lanes for RF DAC**
- **8 transmit lanes for RF ADC**
- **204B compatible with the maximum 15.5 Gbps lane rate**
- **204C compatible with the maximum 24.75 Gbps lane rate**
- **Sample/bit repeat mode for receive lane rate matching**

(*Id.* at 1.)

FEATURES

Flexible reconfigurable radio common platform design
- **4D2A (4 × 3 GSPS to 12 GSPS DAC and 2 × 3 GSPS to 6 GSPS ADC)**
- **4D1A (4 × 3 GSPS to 12 GSPS DAC and 1 × 3 GSPS to 6 GSPS ADC)**
- **RF DAC/RF ADC output/input −3 dB bandwidth of 5.2 GHz and 7.5 GHz**
- **Transmit/receive channel bandwidth up to 1.6 GHz/3 GHz (4T2R)**
- **Transmit/receive channel bandwidth up to 2.4 GHz/3 GHz (2T2R)**
- **On-chip PLL (6 GHz to 12 GHz) with multichip synchronization; output clock provided**
- **External RFCLK input option**

(*Id.*)

60. The AD9082 is a transceiver that is designed to be connected to a data source and a data receiver. As shown in Figure 1 of the AD9082 data sheet (reproduced above), the AD9082 includes various data input pins (to be connected with a data source) as well as data output pins (to be connected with a data receiver).

61. The AD9082 includes an input port for accepting a control signal having a first and a second state. Specifically, the AD9082 data sheet at page 1 provides that the transceiver is configurable to operate at different lane rates (JESD204B compatible vs. JESD204C compatible). (Exhibit 11 at 1.) In order to configure the AD9082 transceiver in one of these two state, it is necessary to accept a control signal from an input port to effect the configuration.

62. The AD9082 includes a serializer designed to operate at first data rate. For example, in one state of operation, the input JESD204 serializer of the AD9082 provides a lane rate of 15.5 Gbps. (Exhibit 11 at 1.)

63. The AD9082 includes a first interface that receives a first set of data from the data source at a second data rate and delivers a second set of data to the serializer at the first data rate, the second data rate being lower than the first data rate when the control signal is at the first state and the second rate being same as the first data rate when the control signal is at the second state. Specifically, the AD9082 includes a JESD204 interface (either 204B or 204C compatible) that is capable of being configured to operate in sample/bit repeat mode to match the receive lane rate, which in the JESD204B compatible state is a slower rate than the maximum lane rate of the AD9082.

64. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the ’767 patent, including at least claim 1, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing in the United States the ’767 Infringing Products.

65. At least as of the filing of this Counterclaim, ADI has knowledge of the ’767 patent.

66. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the ’767 patent, including at least claim 1, under 35 U.S.C. § 271(b) by customers and other end users of the ’767 Infringing Products in the United States. ADI’s acts of inducement include at least selling the ’767 Infringing Products, which are configured to infringe the ’767 patent. These acts actively encourage and induce

customers and other end users of the '767 Infringing Products to directly infringe at least claim 1 of the '767 patent by using the products in the United States.

67. ADI is committing these acts of infringement of the '767 patent without license or authorization.

68. As a result of ADI's infringement of the '767 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

69. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '767 Infringing Products infringe the '767 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '767 patent.

70. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

FOURTH COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 7,116,251

71. Xilinx repeats and incorporates by reference paragraphs 1-70 of these Counterclaims as if fully set forth herein.

72. The '251 patent was duly and legally issued by the PTO on October 3, 2006, and is titled "Programmable Serializing Data Path."

73. Xilinx possesses all ownership rights, title, and interests in the '251 patent.

74. ADI has infringed, currently infringes, and will continue to infringe at least claim 1 of the '251 patent. AD9208 is representative of infringement by the '251 Infringing Products.

75. Claim 1 of the '251 patent states:

A method for programmable serializing of parallel data, the method comprises:

receiving the parallel data;

obtaining a data width of the parallel data, wherein the data width is of a first multiple or a second multiple;

obtaining a desired serial data output rate;

generating a multiple state control sequence based on the data width of the parallel data and the desired serial data output rate; and

converting the parallel data into serial data in accordance with the multiple state control sequence.

76. Relevant excerpts from the AD9208 data sheet, attached as Exhibit 10, are reproduced above under Xilinx's Third Counterclaim (ADI's Infringement of U.S. Patent No. 7,015,838 patent). (Exhibit 10 at 67-71.)

77. The AD9208 performs a method for programmable serializing of parallel data, as discussed below.

78. The AD9208 receives parallel data. For example, Figure 107 of the AD9208 data sheet (Exhibit 10 at 68, reproduced above) illustrates parallel data received by the JESD204B serializer.

79. The AD9208 performs the step of obtaining a data width of the parallel data, wherein the data width is of a first multiple or a second multiple. For example, as shown in Table 46 of the AD9208 data sheet (Exhibit 10 at 117, reproduced above), register 0x085F, bits 4:0, configures the converter resolution that dictates the data width output of a converter. Various multiples of data width are configurable.

80. The AD9208 performs the step of obtaining a desired serial data output rate. For example, Table 31 of the AD9208 data sheet shows different lane rates that can be contained. (Exhibit 10 at 70.)

81. The AD9208 performs the step of generating a multiple state control sequence based on the data width of the parallel data and the desired serial data output rate. For example, the AD9208 phase-locked loop generates a serial data clock having a rate corresponding to the desired serial data output rate, as shown in Table 31 of the AD9208 data sheet (Exhibit 10 at 70, reproduced above), wherein the lane rate is depending upon the data width, as shown by the Lane Rate equation on p. 72 of the AD9208 data sheet (*Id.*). Footnote 3 of Table 33 of the AD9208 data sheet further clarifies that the serial lane rate is accomplished by dividing the serial data clock into an intermediate data clock with a frequency that is based on the desired lane rate range, thereby generating multiple state control signals:

[3] f_{ADC_CLK} is the ADC sample rate; DCM = chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 15.5 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 15500 Mbps and > 13500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

(*Id.* at 73.)

82. Finally, the AD9208 performs the step of converting the parallel data into serial data in accordance with the multiple state control sequence. For example, the JESD204B serializer as shown in Figure 107 of the AD9208 data sheet (Exhibit 10 at 68) converts the received parallel data into serial data, in accordance with the multiple state control sequence discussed above.

83. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the ’251 patent, including at least claim 1, literally or under the doctrine of equivalents,

under 35 U.S.C. § 271(a) by using the '251 Infringing Products. Such infringing use by ADI occurs, for example, when ADI tests the '251 Infringing Products.

84. At least as of the filing of this Counterclaim, ADI has knowledge of the '251 patent.

85. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '251 patent, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing the '251 Infringing Products in the United States. For example, ADI has directly infringed at least claim 1 by using the '251 Infringing Products in the United States, including for testing purposes.

86. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '251 patent, including at least claim 1 under 35 U.S.C. § 271(b) by customers and other end users of the '251 Infringing Products in the United States. ADI's acts of inducement include at least selling the '251 Infringing Products, including evaluation board products. These acts actively encourage and instruct customers and other end users of the '251 Infringing Products to directly infringe in the United States at least claim 1 of the '251 patent.

87. ADI is committing these acts of infringement of the '251 patent without license or authorization.

88. As a result of ADI's infringement of the '251 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

89. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '251 Infringing Products infringe the '251 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '251 patent.

90. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

FIFTH COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 7,187,709

91. Xilinx repeats and incorporates by reference paragraphs 1-90 of these Counterclaims as if fully set forth herein.

92. The '709 patent was duly and legally issued by the PTO on March 6, 2007, and is titled "High Speed Configurable Transceiver Architecture."

93. Xilinx possesses all ownership rights, title, and interests in the '709 patent.

94. ADI has infringed, currently infringes, and will continue to infringe at least claim 8 of the '709 patent. ADRV9009 is representative of infringement by the '709 Infringing Products.

95. Claim 8 of the '709 patent states:

> An integrated circuit comprising:
>
> a programmable fabric;
>
> a processor core surrounded by said programmable fabric;
>
> a plurality of configurable transceivers located at the peripheral of said programmable fabric, wherein at least one of said configurable transceivers comprises a loss of synchronization detector;

wherein each transceiver has an input port that receives differential input signals and an output port that outputs differential output signals; and

wherein each configurable transceiver includes a configurable serializer and a configurable deserializer, wherein each serializer is configurable to transmit data at a selected bit rate, and each deserializer is configurable to receive data at the selected bit rate;

a plurality of signal paths connecting at least one of said configurable transceivers and said processor core, at least a portion of each of said signal paths passing through said programmable fabric.

96. Excerpts from the ADRV9009 data sheet, attached as Exhibit 12, are reproduced below:

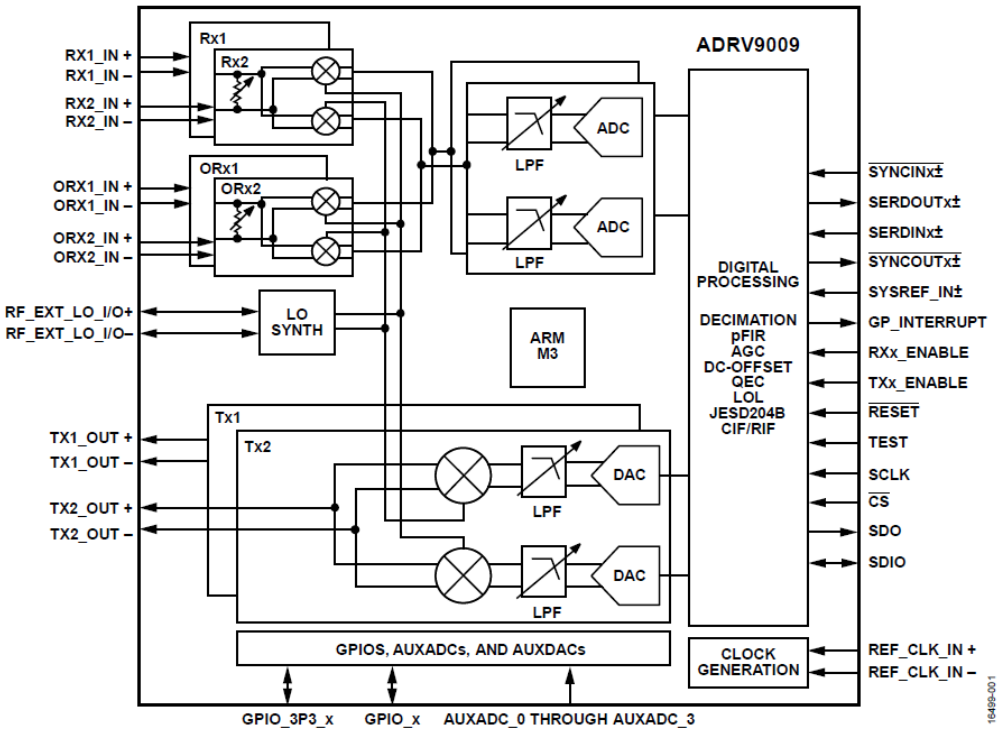


Figure 1.

(Exhibit 12 at 4.)

TRANSMITTER

The ADRV9009 transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the JESD204B lanes pass through a fully programmable, 128-tap FIR filter with variable interpolation rates. The FIR output is sent to a series of interpolation filters that provide additional filtering and interpolation prior to reaching the DAC. Each 14-bit DAC has an adjustable sample rate.

(*Id.* at 98.)

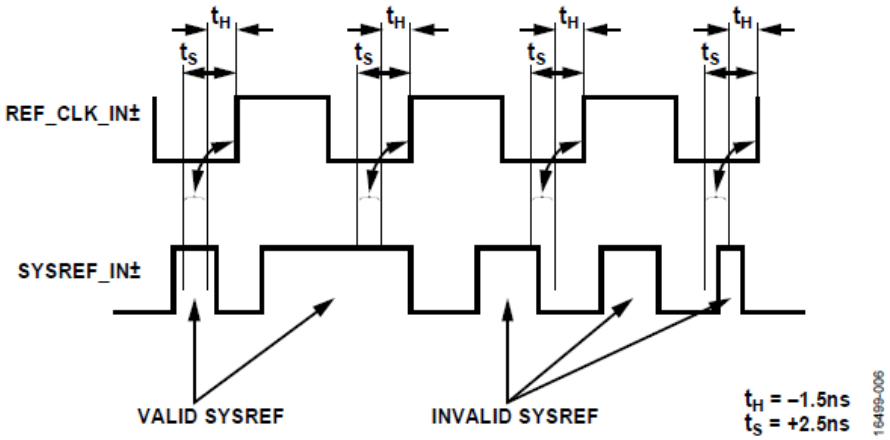


Figure 3. SYSREF_IN± Setup and Hold Timing Examples, Relative to Device Clock

(*Id.* at 15.)

JESD204B DATA INTERFACE

The digital data interface for the ADRV9009 uses JEDEC JESD204B Subclass 1. The serial interface operates at speeds of up to 12.288 Gbps. The benefits of the JESD204B interface include a reduction in required board area for data interface routing, resulting in smaller total system size. Four high speed serial lanes are provided for the transmitter and four high speed lanes are provided for the observation receiver. The ADRV9009 supports single-lane or dual-lane interfaces as well as fixed and floating point data formats for observation receiver data.

Table 6. Observation Path Interface Rates

Bandwidth (MHz)	Output Rate (MSPS)	JESD204B	
		Lane Rate (Mbps)	Number of Lanes
200	245.76	9830.4	1
200	307.2	12288	1
250	307.2	12288	1
450	491.52	9830.4	2
450	491.52	4915.2	4

(*Id.* at 99.)

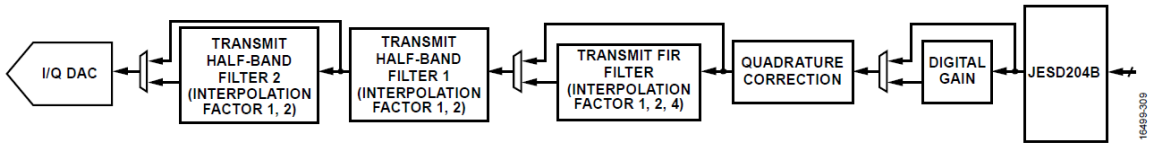


Figure 430. Transmitter Datapath Filter Implementation

(*Id.* at 100.)

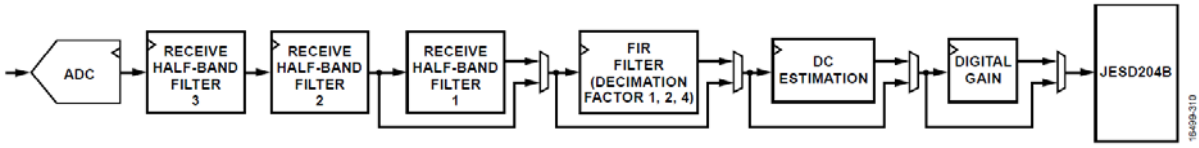


Figure 431. Receiver and Observation Receiver Datapath Filter Implementation

(*Id.*)

97. The ADRV9009 is an integrated circuit.

98. The ADRV9009 includes a programmable fabric. For example, the ADRV9009 includes a fully programmable128-tap FIR filter, as discussed on page 98 of the ADRV9009 data sheet. (Exhibit 12 at 98.)

99. On information and belief, the ADRV9009 includes a processor core surrounded by said programming fabric. For example, as shown in Figure 1 of the ADRV9009 data sheet (Exhibit 12 at 4), the digital processing module, includes a processor core.

100. The ADRV9009 includes a plurality of configurable transceivers located at the peripheral of said programmable fabric, wherein at least one of said configurable transceivers comprises a loss of synchronization detector. For example, Figure 1 of the ADRV9009 data sheet (Exhibit 12 at 4) shows the digital processing function block receiving and outputting signals, including receiving differential SYSREF_IN signals. Page 99 of the ADRV9009 data sheet (Exhibit 12) confirms that the JESD204B interface includes transceivers that are configurable, as further illustrated in Table 6 (reproduced above). Finally, Figure 3 of the ADRV9009 data sheet (*Id.* at 15) shows a that the SYSREF_IN transceiver includes a loss of synchronization detector that detects the loss of synchronization of the SYSREF_IN signals with respect to a device clock signal and (and classifies it as invalid).

101. The above said transceivers in the ADRV9009 each have an input port that receives differential input signals and an output port that outputs differential output signals. For example, Figure 1 of the ADRV9009 data sheet shows the digital processing block (which includes the JESD204B interface) receiving and outputting differential signals, including the SYNCIN, SYNCOUT, and SYSREF_IN differential signals. (Exhibit 12 at p. 4.)

102. In the ADRV9009, each configurable transceiver includes a configurable serializer and a configurable deserializer, wherein each serializer is configurable to transmit data

at a selected bit rate, and each deserializer is configurable to receive data at the selected bit rate. For example, Figure 1 of the ADRV9009 data sheet shows the digital processing block to include a JESD204B serializer/deserializer interface. (Exhibit 12 at 4.) Furthermore, Table 6 of the ADRV9009 data sheet (*Id.* at 99) shows the JESD204B serializer/deserializer interface to be configurable to transmit data at a selected bit rate.

103. Finally, the ADRV9009 includes a plurality of signal paths connecting at least one of said configurable transceivers and said processor core, at least a portion of each of said signal paths passing through said programmable fabric. For example, as shown in Figures 430 and 431 of the ADRV9009 data sheet (Exhibit 12 at 100), signal paths connect between the configurable transceivers to processor cores through the FIR programmable fabric.

104. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '709 patent, including at least claim 1, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing in the United States the '709 Infringing Products.

105. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '709 patent, including at least claim 1 under 35 U.S.C. § 271(b) by customers and other end users of the '709 Infringing Products in the United States. ADI's acts of inducement include at least selling the '709 Infringing Products, including evaluation board products. These acts actively encourage and instruct customers and other end users of the '709 Infringing Products to directly infringe in the United States at least claim 1 of the '709 patent.

106. At least as of the filing of this Counterclaim, ADI has knowledge of the '709 patent.

107. ADI is committing these acts of infringement of the '709 patent without license or authorization.

108. As a result of ADI's infringement of the '709 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

109. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '709 Infringing Products infringe the '709 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '709 patent.

110. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

SIXTH COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 7,224,184

111. Xilinx repeats and incorporates by reference paragraphs 1-110 of these Counterclaims as if fully set forth herein.

112. The '184 patent was duly and legally issued by the PTO on May 29, 2007, and is titled "High Bandwidth Reconfigurable On-Chip Network for Reconfigurable Systems."

113. Xilinx possesses all ownership rights, title, and interests in the '184 patent.

114. ADI has infringed, currently infringes, and will continue to infringe at least claim 1 of the '184 patent. AD9208 is representative of infringement by the '184 Infringing Products.

115. Claim 1 of the '184 patent states:

A programmable logic device (PLD) comprising:

modules for implementing tasks, the modules being reconfigurable; and

a crossbar switch providing communication paths between the modules, the crossbar switch being dynamically reconfigurable while communication occurs over a portion of the crossbar switch between modules.

116. Excerpts from pages 40-41 of the AD9208 data sheet, attached as Exhibit 10, are reproduced below:

DDC I/Q INPUT SELECTION

The AD9208 has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real and complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x0311, Register 0x0331, Register 0x0351, and Register 0x0371). See Table 46 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real and complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit, Bit 3, in the DDC control registers (Register 0x0310, Register 0x0330, Register 0x0350, and Register 0x0370).

The chip Q ignore bit in the chip mode register (Register 0x0200, Bit 5) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 101.

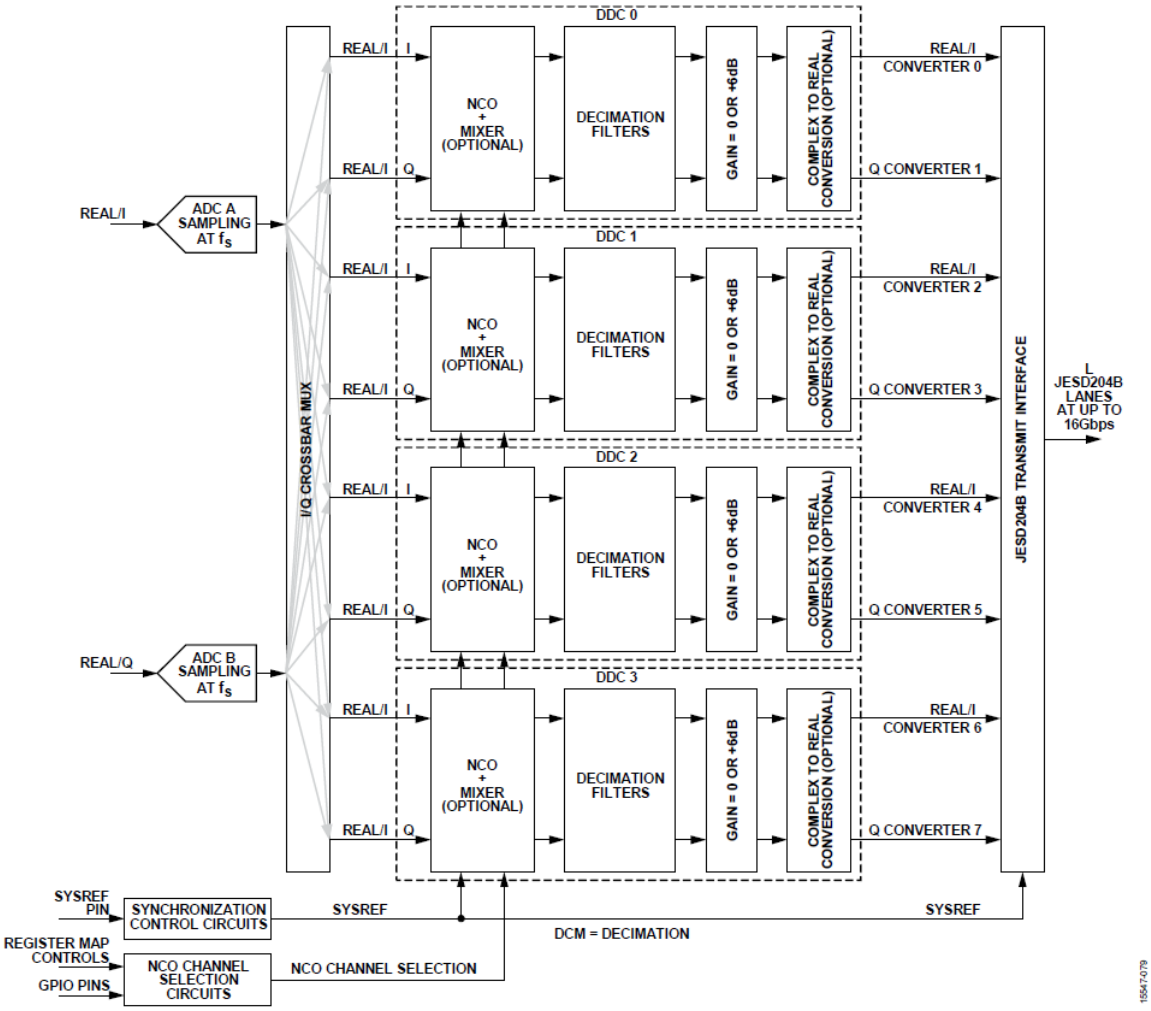


Figure 84. DDC Detailed Block Diagram

117. The AD9208 includes a programmable logic device. Specifically, as shown above, the AD9208 includes circuitry with digital down converters (DDC) that make up a programmable logic device.

118. The AD9208 includes modules for implementing tasks, the modules being reconfigurable. For instance, as shown above in the excerpts, the AD9208 includes ADC modules and DDC modules. The modules are reconfigurable to output either real data or complex output data from the DDCs.

119. The AD9208 includes a crossbar switch (*i.e.*, a crossbar MUX) providing communication paths between the modules, the crossbar switch being dynamically reconfigurable while communication occurs over a portion of the crossbar switch between modules. For instance, the AD9208 can be configured such that the DDC inputs can be set to receive data from either ADC Chanel A or ADC Chanel A as well as ADC Chanel B. In response to the DDC input configuration, the crossbar switch is dynamically reconfigured while communication occurs over a portion of the crossbar switch between modules.

120. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '184 patent, including at least claim 1, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing in the United States the '184 Infringing Products.

121. At least as of the filing of this Counterclaim, ADI has knowledge of the '184 patent.

122. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '184 patent, including at least claim 1, under 35 U.S.C. § 271(b) by customers and other end users of the '184 Infringing Products in the United States. ADI's acts of inducement include at least selling the '184 Infringing Products. These acts actively encourage and instruct customers and other end users of the '184 Infringing Products to directly infringe in the United States at least claim 1 of the '184 patent.

123. ADI is committing these acts of infringement of the '184 patent without license or authorization.

124. As a result of ADI's infringement of the '184 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

125. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '184 Infringing Products infringe the '184 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '184 patent.

126. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

SEVENTH COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 7,280,590

127. Xilinx repeats and incorporates by reference paragraphs 1-126 of these Counterclaims as if fully set forth herein.

128. The '590 patent was duly and legally issued by the PTO on October 9, 2007, and is titled "Receiver Termination Network And Application Thereof."

129. Xilinx possesses all ownership rights, title, and interests in the '590 patent.

130. ADI has infringed, currently infringes, and will continue to infringe at least claim 1 of the '590 patent. AD9174 is representative of infringement by the '590 Infringing Products.

131. Claim 1 of the '590 patent states:

A high-speed receiver comprising:

a receiver termination network that includes:

a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed data via the transmission line; and

an AC coupled bias circuit operably coupled to provide a common mode reference and to high pass filter the high-speed data to produce the filtered high-speed data;

a receiver analog front-end biased in accordance with the common mode reference, wherein the receiver analog front-end is operably coupled to amplify the filtered high-speed data to produce amplified high-speed data; and

a data recovery module operably coupled to recover data from the amplified high-speed data.

132. Excerpts from the page 42 of the AD9174 data sheet, attached as Exhibit 13, are reproduced below:

The AD9174 supports a periodic SYSREF± signal. The periodicity can be continuous, strobed, or gapped periodic. The SYSREF± signal can be dc-coupled with a common-mode voltage of 0.6 V to 2.2 V and differential swing of 200 mV p-p to 1 V p-p. When dc-coupled, a small amount of common-mode current (up to 0.3 mA) is drawn from the SYSREF± pins. See Figure 61 and Figure 62 for the SYSREF± internal circuit for dc-coupled and a c-coupled configurations. Ensure that the SYSREF_INPUTMODE bit (Register 0x084, Bit 6) is set to 1, dc-coupled, to prevent overstress on the SYSREF± receiver pins.

To avoid this common-mode current draw, the SYSREF± receiver can be ac-coupled using a 50% duty cycle periodic SYSREF± signal with ac coupling capacitors. If ac-coupled, the ac coupling capacitors combine with the resistors shown in Figure 62 to make a high-pass filter with an RC time constant of $\tau = RC$.

By default, the first SYSREF± rising edge at the SYSREF± inputs that is detected after asserting the SYSREF_MODE_ONESHOT bit (Register 0x03A, Bit 1) begins the synchronization and aligns the internal LMFC signal with the sampled SYSREF± edge.

Register 0x036 (SYSREF_COUNT) indicates how many captured SYSREF± edges are ignored after the SYSREF_MODE_ONESHOT bit is asserted before the synchronization takes place. For example, if SYSREF_COUNT is set to 3, the AD9174 does not sync after the SYSREF_MODE_ONESHOT bit is asserted until the arrival of the 4th SYSREF± edge.

(Exhibit 13 at 42.)

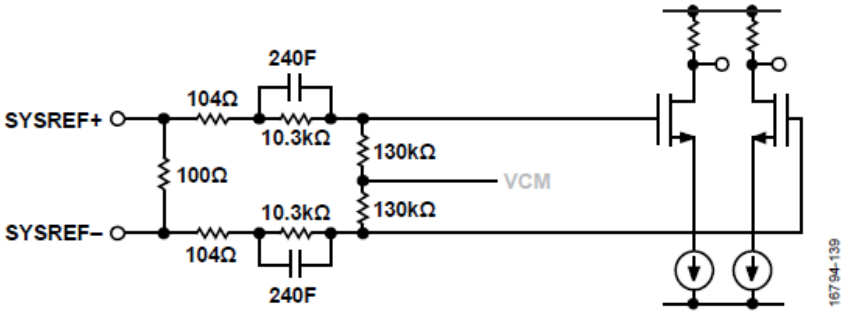


Figure 62. AC-Coupled SYSREF± Receiver Circuitry

(*Id.* at 42.)

133. The AD9174 includes a high-speed receiver. Specifically, the AD9174 includes a receiver termination network for receiving the SYSREF data, which is received at a rate controlled by a clock source operating in GHz range (*see* Exhibit 13 at 42); GHz rate of speed is considered high speed at the time of the '590 patent.

134. The AD9174 includes a receiver termination network that includes a DC matched termination circuit operably coupled to provide a termination of a transmission line coupling the high-speed receiver to a transmission source and to receive high-speed data via the transmission line, and an AC coupled bias circuit operably coupled to provide a common mode reference and to high pass filter the high-speed data to produce the filtered high-speed data. Specifically, referring to Figure 62 of the AD9174 data sheet, the 100Ω resistor makes up the DC matched termination circuit that is operatively coupled to provide a termination of the received SYSREF data. (Exhibit 13 at 42.) The termination network also includes a pair of RC circuits that is AC coupled to provide a common mode reference and to act as a high-pass filter, as explained in the AD9174 data sheet (excerpt reproduced above). (*Id.*)

135. The above-illustrated termination circuit of the AD9174 also includes a receiver analog front-end biased in accordance with the common mode reference, wherein the receiver analog front-end is operably coupled to amplify the filtered high-speed data to produce amplified high-speed data. Specifically, Figure 62 illustrates an analog front end that is biased in accordance with VCM, and is operatively coupled to amplify the high-pass filter data from the above-referenced pair of RC circuits. (Exhibit 13 at 42.)

136. Finally, the above-referenced termination network of the AD9174 also includes a data recovery module operably coupled to recover data from the amplified high-speed data. Specifically, the termination network outputs the amplified SYSREF data to be sampled.

137. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '590 patent, including at least claim 1, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing in the United States the '590 Infringing Products.

138. At least as of the filing of this Counterclaim, ADI has knowledge of the '590 patent.

139. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '590 patent, including at least claim 1, under 35 U.S.C. § 271(b) by customers and other end users of the '590 Infringing Products in the United States. ADI's acts of inducement include at least selling the '590 Infringing Products. These acts actively encourage and instruct customers and other end users of the '590 Infringing Products to directly infringe in the United States at least claim 1 of the '590 patent.

140. ADI is committing these acts of infringement of the '590 patent without license or authorization.

141. As a result of ADI's infringement of the '590 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

142. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '590 Infringing Products infringe the '590 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '590 patent.

143. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

EIGHTH COUNTERCLAIM

ADI'S INFRINGEMENT OF U.S. PATENT NO. 8,548,071

144. Xilinx repeats and incorporates by reference paragraphs 1-143 of these Counterclaims as if fully set forth herein.

145. The '071 patent was duly and legally issued by the PTO on October 1, 2013, and is titled "Integrated Circuit Enabling the Communication of Data and a Method of Communicating Data in an Integrated Circuit."

146. Xilinx possesses all ownership rights, title, and interests in the '071 patent.

147. ADI has infringed, currently infringes, and will continue to infringe at least claim 14 of the '071 patent and, upon information and belief, also claim 15 of the '071 patent. AD9625 is representative of infringement by the '071 Infringing Products.

148. Claim 14 of the '071 patent states:

> A method of communicating data with an integrated circuit, the method comprising:
>
> implementing a plurality of analog-to-digital converter circuits in the integrated circuit;
>
> coupling an analog input signal to the integrated circuit; and
>
> sampling, by the plurality of analog-to-digital converter circuits, the analog input signal received at an input/output port.

149. Claim 15 of the '071 patent states:

> The method of claim 14 further comprising configuring programmable interconnect circuits coupled between the input/output port of the integrated circuit and the plurality of analog-to-digital converter circuits of the integrated circuit.

150. AD9625 performs the method recited in claim 14 of the '071 patent.

151. AD9625 performs a method of communicating data with an integrated circuit. Below is a functional block diagram from ADI's data sheet for AD9625, which is attached hereto as Exhibit 14. The diagram shows that a differential input signal (VIN+ and VIN-) is communicated with the integrated circuit through an ADC core.

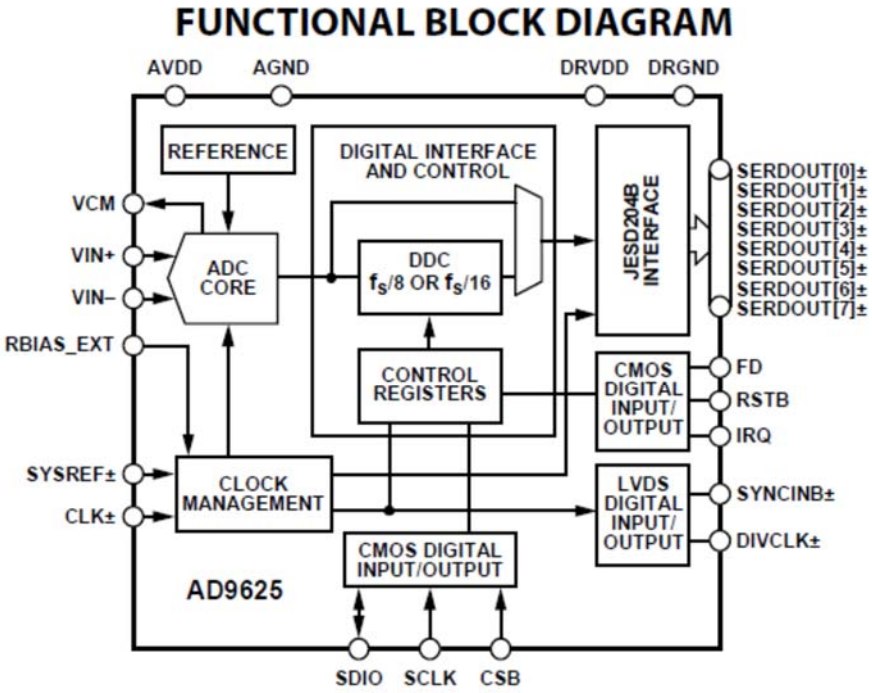


Figure 1.

(Exhibit 14 at 1.)

152. AD9625 implements a plurality of analog-to-digital converter circuits in the integrated circuit. Attached hereto as Exhibit 15 is an ADI article retrieved from ADI's website at https://www.analog.com/media/en/analog-dialogue/volume-49/number-3/articles/interleaving-adcs.pdf on January 19, 2020 ("ADI Interleaving Article", July 2015). The article states: "The AD9625 is a 12-bit/2.5 GSPS three-way interleaved ADC." (Exhibit 15 at 3.) An interleaved ADC, by definition, has a plurality of analog-to-digital converter circuits. This is verified by Figure 1 of the ADI Interleaving Article, which is reproduced below. Figure 1 of the ADI

Interleaving Article shows an interleaved ADC composed of M sub-ADCs, where M is greater than 1.

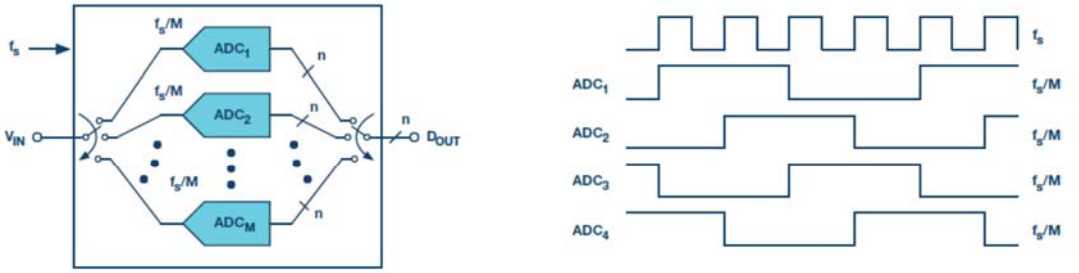


Figure 1. An array of M time interleaved n-bit ADCs. The sample rate of each one is f_S/M, the resulting sample rate of the time interleaved ADCs is f_S. An example of clocking scheme for the case of M = 4 is depicted on the lower part of this figure.

(Exhibit 15, Fig. 1.)

153. AD9625 couples an analog input signal to the integrated circuit. In the functional block diagram above, the differential input signal (VIN+ and VIN-) is coupled to the ADC core. (Exhibit 15 at 1.) Because the ADC converts analog signals to digital signals, the input signal is an analog signal.

154. AD9625 samples, by the plurality of analog-to-digital converter circuits, the analog input signal received at an input/output port. This follows from ADI's characterization of AD9625 in the ADI article as an "interleaved ADC." For example, the ADI article states: "To better understand the principle of IL [interleaving], in Figure 1 an analog input VIN(t) is sampled by the M ADCs and results in a combined digital output data series DOUT." (Exhibit 15 at 1.) Correspondingly, in the block diagram above, the differential input signal (VIN+ and VIN-) is sampled by the plurality of ADCs making up the ADC core. (*Id.*)

155. Upon information and belief, AD9625 also performs the method recited in claim 15.

156. Upon information and belief, AD9625 configures programmable interconnect circuits between the input/output port of the integrated circuit and the plurality of analog to

digital converter circuits of the integrated circuit. United States Patent No. 9,793,910 (the "'910 patent"), entitled "Time-Interleaved ADCs with Programmable Phases," was granted to ADI on October 17, 2017. ADI's '910 patent states:

> In some cases, the adjustment of the duration of one or more phases is triggered based on a characteristic of the analog input signal. Performance of the sub-ADC can often change based on characteristics such as frequency, amplitude, or amount of noise in the analog-input signal. If a characteristic of the analog input signal can negatively affect a particular performance metric, it may be desirable to compensate for the loss in that performance metric (or to make up for the loss by increasing another performance metric) by adjusting duration of one or more phases. The control signal to the phase controller 406 can reflect such tradeoff and cause the phase controller 406 to change the duration of one or more phases. To sense a characteristic of the analog input signal, circuitry (e.g., a sensing ADC) can be included to directly sense the analog input signal, or indirectly sense the analog input signal by processing any one or more of the following: digital signals in the sub-ADCs and digital output signals . . . . The phase controller 406 adjusts duration of one or more phases based on a characteristic of the analog input signal (e.g., a mode of operation having the desired tradeoff can be reflected in the control signal being provided to phase controller 406).

(Exhibit 16 at 7:1-23.)

157. Figure 4 of ADI '910 patent is reproduced below.

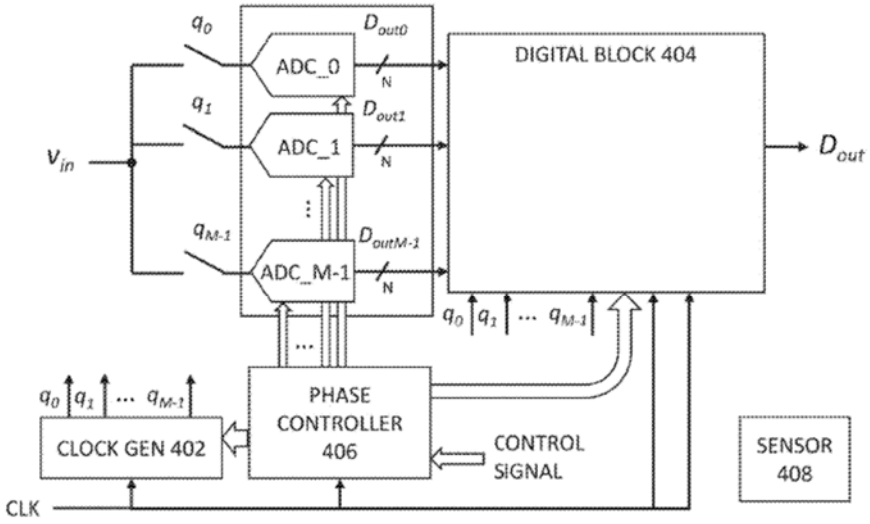


FIGURE 4

(Exhibit 16 at Fig. 4.)

158. The phase controller 406, clock generator 402, and plurality of switches (designated q0 through qM-1) in Figure 4, as described at Column 7, lines 1 through 23 of ADI's '910 patent, make up a programmable interconnect circuit. Upon information and belief, AD9625 employs this circuit or a substantially similar circuit.

159. ADI has infringed, currently infringes, and will continue to infringe one or more claims of the '071 patent, literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) at least by making, using, selling, offering for sale, and/or importing the '071 Infringing Products in the United States. For example, ADI has directly infringed at least claim 14 and, upon information and belief, claim 15 by using the '071 Infringing Products in the United States, including for testing purposes.

160. At least as of the filing of this Counterclaim, ADI has knowledge of the '071 patent.

161. ADI has actively induced, currently actively induces, and will continue to actively induce the infringement of one or more claims of the '071 patent, including at least claim 14 and, upon information and belief, claim 15, under 35 U.S.C. § 271(b) by customers and other end users of the '071 Infringing Products in the United States. ADI's acts of inducement include at least selling the '071 Infringing Products and publishing and disseminating the ADI Interleaving Article. These acts actively encourage and instruct customers and other end users of the '071 Infringing Products to directly infringe in the United States at least claim 14 and, upon information and belief, claim 15 of the '071 patent.

162. ADI is committing these acts of infringement of the '071 patent without license or authorization.

163. As a result of ADI's infringement of the '071 patent, Xilinx has suffered damages and will continue to suffer damages, including damages awardable under 35 U.S.C. §§ 284 and 285.

164. At least as early as ADI's receipt of this Counterclaim, ADI knew or was willfully blind to how the '071 Infringing Products infringe the '071 patent. ADI has engaged and continues to engage in willful and deliberate infringement of the '071 patent.

165. ADI's infringing conduct has caused and is causing irreparable harm to Xilinx for which Xilinx has no adequate remedy at law, and such irreparable harm will continue unless and until ADI is enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Xilinx respectfully requests that this Court enter judgment in its favor and against ADI and grant the following relief:

A. Judgment that Xilinx, Inc. has not and does not infringe, whether directly, or indirectly, literally or under the doctrine of equivalents, any valid and enforceable claim of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents;

B. Judgment that the claims of the '452, '518, '750, '250, '321, '463, '659, and '075 Patents are invalid and/or unenforceable;

C. Dismissal of all of ADI's claims against Xilinx, Inc. in their entirety and with prejudice;

D. Judgment that ADI take nothing by way of its Complaint;

E. Judgment that one or more of the Accused ADI Products infringes one or more claims of the Xilinx Patents;

F. A preliminary injunction prohibiting ADI, its officers, agents, servants, employees, attorneys, and affiliated companies, its assigns and successors in interest, and those

persons in active concert of participation with ADI, from continued acts of infringement of the Xilinx Patents;

G. A permanent injunction prohibiting ADI, its officers, agents, servants, employees, attorneys, and affiliated companies, its assigns and successors in interest, and those persons in active concert of participation with ADI, from continued acts of infringement of the Xilinx Patents;

H. Awarding Xilinx damages adequate to compensate it for ADI's infringing activities, including supplemental damages for any post-verdict infringement up until entry of the final judgment with an accounting as needed, together with pre-judgment and post-judgment interest on the damages awarded;

I. Finding ADI's infringement to be willful and awarding enhanced damages in an amount up to treble the amount of compensatory damages as justified under 35 U.S.C. § 284;

J. An order awarding Xilinx its costs pursuant to 35 U.S.C. § 284 and/or Rule 54(d) of the Federal Rules of Civil Procedure;

K. An order finding this an exceptional case, and awarding Xilinx its costs, expenses, and reasonable attorney fees under 35 U.S.C. § 285 and all other applicable statutes and rules in common law as may apply; and

L. An order awarding Xilinx such further relief as the Court may deem appropriate under the circumstances.

JURY TRIAL DEMAND

Pursuant to Fed. R. Civ. P. 38(b) and D. Del. LR 38.1, Xilinx hereby demands a trial by jury on all issues triable by a jury as of right in this action.

Dated: January 21, 2020

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CERTIFICATE OF SERVICE

I, Anne Shea Gaza, hereby certify that on January 21, 2020, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

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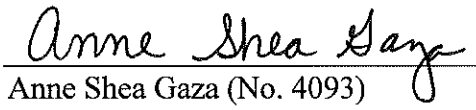
I further certify that on January 21, 2020, I caused the foregoing document to be served via electronic mail upon the above-listed counsel and on the following counsel:

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