No. 2022-1906

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VLSI TECHNOLOGY LLC,

Plaintiff-Appellee,

v.

INTEL CORPORATION,

Defendant-Appellant.

On Appeal from the United States District Court for the Western District of Texas in Case No. 6:21-cv-00057-ADA, Judge Alan D. Albright

NON-CONFIDENTIAL BRIEF FOR DEFENDANT-APPELLANT INTEL CORPORATION

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September 14, 2022

PATENT CLAIMS AT ISSUE

Claim 1 of the ’373 Patent

1. A method, comprising:

providing an integrated circuit with a memory;

operating the memory with an operating voltage;

determining a value of a minimum operating voltage of the memory;

providing a non-volatile memory (NVM) location;

storing the value of the minimum operating voltage of the memory in the NVM location;

providing a functional circuit on the integrated circuit exclusive of the memory;

providing a first regulated voltage to the functional circuit;

providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;

providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and

providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

Appx111(13:7-28).

Claim 14 of the ’759 Patent

14. A system comprising:

a bus capable of operation at a variable clock frequency;

a first master device coupled to the bus, the first master device configured to provide a request to change a clock frequency of a high-speed clock in response to a pre-defined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

a programmable clock controller having an embedded computer program therein, the computer program including instructions to:

receive the request provided by the first master device;

provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device; and

provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

Appx123-124(8:50-9:4).

CERTIFICATE OF INTEREST

Counsel for Defendant-Appellant Intel Corporation certifies the following:

1. Represented Entities. Fed. Cir. R. 47.4(a)(1). Provide the full names of all entities represented by undersigned counsel in this case.

Intel Corporation.

2. Real Party in Interest. Fed. Cir. R. 47.4(a)(2). Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.

None.

3. Parent Corporations and Stockholders. Fed. Cir. R. 47.4(a)(3). Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.

None.

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

WILMER CUTLER PICKERING HALE AND DORR LLP: Arthur W. Coviello, Jeffrey A. Dennhardt, Felicia H. Ellsworth, Jordan L. Hirsch, Thomas Lampert, Gregory H. Lantier, James M. Lyons, George F. Manley, Alexis Pfeiffer, Kate Saxton, Joshua L. Stern, Louis W. Tompros, Anh-Khoa Tran, Paul T. Vanderslice

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PILLSBURY WINTHROP SHAW PITTMAN LLP: Brian C. Nash (former)

KIRKLAND & ELLIS LLP: John C. O'Quinn

James Eric Wren, III

5. Related Cases. Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). *See also* Fed. Cir. R. 47.5(b).

VLSI Technology LLC v. Intel Corp., No. 6:21-cv-00299-ADA (W.D. Tex.) (formerly No. 6:19-cv-00255-ADA);

VLSI Technology LLC v. Intel Corp., No. 6:19-cv-00977-ADA (W.D. Tex.) (formerly No. 6:19-cv-256-ADA);

VLSI Technology LLC v. Intel Corp., No. 1:18-cv-966-CFC (D. Del.);

VLSI Technology LLC v. Intel Corp., No. 5:17-cv-05671-BLF (N.D. Cal.);

Intel Corp. v. Fortress Investment Group, No. 2021-0021-MTZ (Del. Ch.);

OpenSky Industries, LLC v. VLSI Technology LLC, IPR2021-01064 (PTAB);

Patent Quality Assurance, LLC v. VLSI Technology LLC, IPR2021-01229 (PTAB);

Intel Corp. v. VLSI Technology LLC, IPR2022-00366 (PTAB) (joined with IPR2021-01064);

Intel Corp. v. VLSI Technology LLC, IPR2022-00479 (PTAB) (joined with IPR2021-01229).

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None.

Dated: September 14, 2022

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CONFIDENTIAL MATERIAL OMITTED

The material omitted from pages 19, 20, 46, and 52 contains confidential Intel and third-party settlement/licensing information; the material omitted from page 21 contains confidential information regarding a juror; and the material omitted from page 64 contains confidential Intel financial information. The material omitted from Addendum pages Appx3-4 contains confidential Intel and third-party licensing information and confidential material regarding VLSI's CEO from a district court order filed under seal; the material omitted from Addendum pages Appx24, Appx43-46, Appx48, Appx55, Appx63-64, Appx77-78, Appx82-83, and Appx85-90 contains confidential Intel technical information from district court orders filed under seal; and the material omitted from Addendum pages Appx96-97 contains confidential Intel financial information from a district court order filed under seal.

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STATEMENT OF RELATED CASES

This Court previously decided two mandamus petitions in this case: *In re Intel Corporation*, No. 2021-105, 841 F. App'x 192 (Fed. Cir. 2020) (per curiam) (Prost, C.J., Lourie & Chen, JJ.) (granting Intel's mandamus petition and vacating the district court's first order retransferring this case from Austin to Waco for trial); and *In re Intel Corporation*, No. 2021-111, 843 F. App'x 272 (Fed. Cir. 2021) (per curiam) (Prost, C.J., Lourie & Chen, JJ.) (subsequently denying Intel's mandamus petition challenging the district court's second order retransferring this case from Austin to Waco for trial). This Court also previously dismissed the following appeals challenging the PTAB's discretionary decision not to institute *inter partes* review ("IPR") of several patents including the two at issue in this appeal: *Intel Corporation v. VLSI Technology LLC*, Nos. 21-1614, -1616, -1617, 2021 WL 5968443 (Fed. Cir. May 5, 2021) (Prost, C.J., joined by O'Malley & Wallach, JJ.).

The Court's decision in this appeal may directly affect or be directly affected by the following pending cases: *VLSI Technology LLC v. Intel Corporation*, No. 6:21-cv-00299-ADA (formerly No. 6:19-cv-255-ADA) (W.D. Tex.); *VLSI Technology LLC v. Intel Corporation*, No. 1:19-cv-00977-ADA (formerly No. 6:19-cv-256-ADA) (W.D. Tex.); *VLSI Technology LLC v. Intel Corporation*, No. 1:18-cv-966-CFC (D. Del.); *VLSI Technology LLC v. Intel Corporation*, No. 5:17-cv-

05671-BLF (N.D. Cal.); and *Intel Corporation v. Fortress Investment Group, et al.*, No. 2021-0021-MTZ (Del. Ch.).[1]

In addition, the Court's decision in this appeal may directly affect or be directly affected by the following instituted IPR proceedings pending before the Patent Office, which are reviewing the patentability of all claims asserted in this case: *OpenSky Industries, LLC v. VLSI Technology LLC*, IPR2021-01064 (PTAB); *Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2021-01229 (PTAB); *Intel Corporation v. VLSI Technology LLC*, IPR2022-00366 (PTAB) (joined with IPR2021-01064); and *Intel Corporation v. VLSI Technology LLC*, IPR2022-00479 (PTAB) (joined with IPR2021-01229).

Intel is unaware of any other case pending in this Court or any other court that will directly affect or be directly affected by the Court's decision in this appeal.

JURISDICTIONAL STATEMENT

The district court had jurisdiction under 28 U.S.C. §§1331, 1338 and entered final judgment on April 21, 2022. Appx98-100. Intel timely appealed on May 19, 2022. Appx4528-4530. This Court has jurisdiction under 28 U.S.C. §1295(a)(1).

[1] This case and the two others filed by VLSI in the Western District of Texas were all previously consolidated under the caption *VLSI Technology LLC v. Intel Corporation*, No. 1:19-cv-00977-ADA (W.D. Tex.).

INTRODUCTION

This appeal arises from one of several lawsuits filed by VLSI Technology, LLC ("VLSI"), an entity formed by a hedge fund for the sole purpose of buying patents to assert against Intel Corporation ("Intel"). In the U.S. portion of its campaign, VLSI has sought to transform a ***$35 million*** investment—the amount it paid to purchase over 170 patents—into more than ***$22 billion*** in patent litigation damages through unsupported infringement theories and outrageous damages claims. This appeal, which comes after the first trial in VLSI's series of lawsuits, demonstrates how extreme VLSI's scheme is: after a six-day trial in Waco, Texas, a jury found that Intel infringed two old patents that were never practiced by the companies that owned them and awarded ***$2.175 billion*** in damages. That award rests upon multiple errors and cannot be sustained.

To begin with, no reasonable jury could find infringement. For one patent, the literal-infringement verdict is unsupported because Intel's accused memory component can and does operate at a ***lower*** voltage than what VLSI's expert alleged was the claimed "***minimum*** operating voltage." For the other patent, the jury's finding of infringement by equivalents cannot stand because it is barred by prosecution history estoppel and because VLSI's expert provided only conclusory equivalents testimony asserting that, contrary to the claim language, the ***same*** component in Intel's products both sends and receives the claimed "request."

Meanwhile, the entire verdict was tainted by irrelevant and prejudicial damages evidence that never should have been before the jury. On the last trial day, and over Intel's objections, the district court allowed VLSI to introduce six prior agreements where Intel had paid amounts ranging from $200 million to $1.5 billion to settle unrelated litigation and to license hundreds of unrelated patents. There was no dispute that these agreements were ***not comparable*** to a hypothetical license to the asserted patents, as VLSI's own expert admitted. The district court nonetheless allowed VLSI to use the noncomparable agreements to portray Intel as a serial infringer who pays large amounts to license patents in litigation and to urge the jury to award similar amounts here—which is exactly what the jury did.

The district court likewise abandoned its gate-keeping role in allowing VLSI to present an unreliable—and exorbitant—damages model at trial. VLSI's damages expert did not rely on the asserted patents' purchase price or any comparable licenses to determine a reasonable royalty. He instead devised a convoluted, made-for-litigation damages methodology that contravened this Court's precedent in several ways. In particular, VLSI's expert violated apportionment principles by creating a regression model that included ***products and features not accused of infringement*** and by relying on technical inputs purporting to measure the patented features' benefits that were similarly derived using ***non-accused products and features***. VLSI's expert also allocated ***all*** of Intel's incremental profits to VLSI, even though

such profit disgorgement was neither legally nor factually supported. And contrary to the entire market value rule, VLSI's expert prejudicially compared the revenues he deemed attributable to the asserted patents with Intel's ***total accused revenues***.

Adding further error, the district court refused to allow Intel to add a license defense that arose during this litigation following an acquisition made by the hedge fund that formed and controls VLSI. Although Intel moved to amend its answer three months before the trial occurred, the court did not rule on Intel's motion for ***16 months*** and then denied it as untimely and futile. That decision not only unfairly punished Intel for the court's own delay, but also misapprehended the license's plain language.

For these reasons, the judgment should be reversed or at least vacated and remanded.

STATEMENT OF ISSUES

1. Whether the '373 patent infringement judgment should be reversed because no reasonable jury could find that Intel's products literally store or use a "minimum operating voltage" as the claims require.

2. Whether the '759 patent infringement judgment should be reversed because prosecution history estoppel bars VLSI's equivalents theory and no reasonable jury could find that Intel's products satisfy the "request" limitations.

3. Whether a new trial is required because the district court erroneously and prejudicially allowed VLSI to introduce noncomparable Intel settlement agreements.

4. Whether a new trial is also required because the district court erroneously allowed VLSI to: (a) present an unreliable damages theory, which depended on a regression model and technical inputs that included non-accused products and features; (b) seek disgorgement of Intel's profits; and (c) introduce Intel's total accused revenues.

5. Whether the district court abused its discretion by not allowing Intel to add a license defense that arose during the litigation.

STATEMENT OF FACTS

A. VLSI's Serial Lawsuits Against Intel

VLSI was formed in 2016 by Fortress Investment Group LLC ("Fortress"), a New York-based hedge fund represented by VLSI's counsel. Appx3860; Appx4061(9:17-23); Appx4952-4953. Fortress is owned by SoftBank Group Corporation, an international holding company with over $400 billion in assets that runs the world's largest technology fund. Appx3863.

Three days after its formation, VLSI began acquiring patents from NXP Semiconductors ("NXP"). Appx3981-3983. Over the next few years, VLSI purchased more than 170 NXP patents—including the two patents-in-suit—for a

total payment of $35 million. Appx13952-14079; Appx1729-1739. VLSI has just two employees and has never made or sold any products. Appx1685-1687. Its only business has been asserting former NXP patents against Intel.

VLSI initially sued Intel in California and Delaware alleging infringement of thirteen patents. In March 2019, VLSI filed another suit in Delaware adding six patents. One month later, VLSI dismissed the second-filed Delaware suit and refiled it as three actions (with two additional patents) in Texas. This appeal arises from the first Texas case and involves U.S. Patent Nos. 7,523,373 ("'373 patent") and 7,725,759 ("'759 patent").[2]

B. VLSI's Assertion Of The '373 Patent

1. The '373 patent

The '373 patent relates to "a minimum memory operating voltage technique." Appx105(1:6-9). A memory, which stores data, must be provided with a power supply voltage to operate. Appx1383; Appx1914-1916. A "minimum operating voltage" is the ***lowest*** voltage at which the memory can reliably operate (e.g., write, read, or retain data). Appx1403; Appx1917-1920; Appx2730-2731.

The patent describes a technique that involves first determining a memory's "minimum operating voltage" and storing that value. Appx101(abstract). "This

[2] NXP came to own these patents after acquiring Freescale, which had acquired Sigmatel. Appx1299. Sigmatel, Freescale, and NXP never used the claimed inventions in any products. Appx1296-1297; Appx1301-1302; Appx1367-1368.

minimum operating voltage information can then be used in determining when an alternative power supply voltage may be switched to the memory[.]" *Id.*

Figure 1 is shown below:

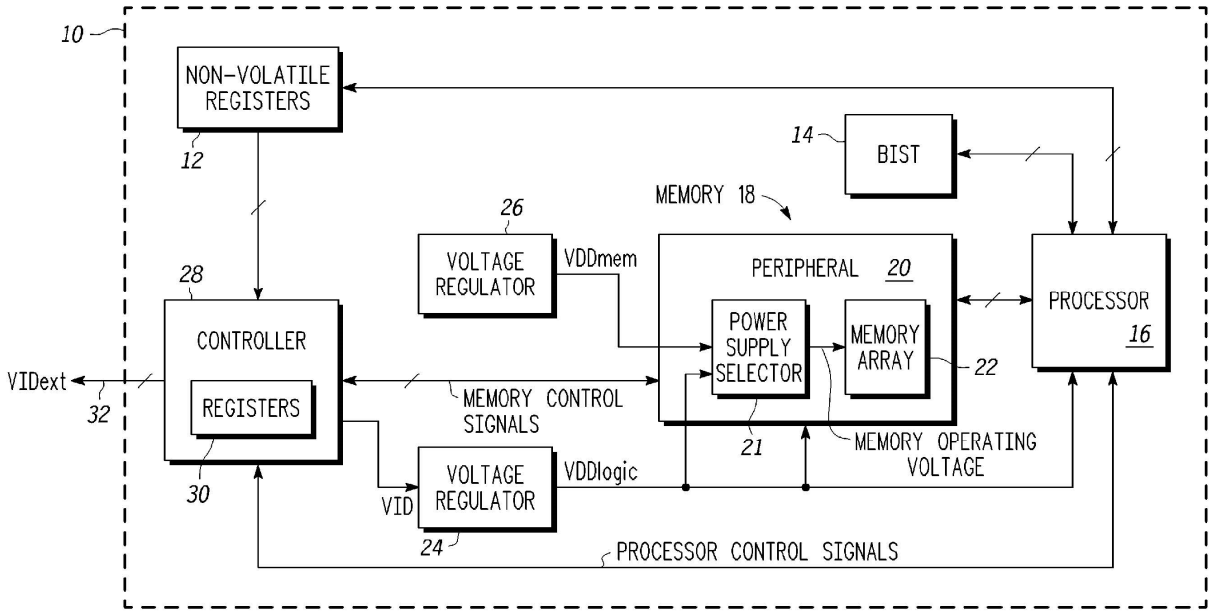


FIG. 1

Appx102. In this embodiment, a minimum operating voltage of memory 18 is stored in registers 12. Appx107(6:30-36). Controller 28 and power supply selector 21 use that stored minimum operating voltage to determine which of two regulated voltages (VDDmem or the lower VDDlogic) to supply to the memory as its operating voltage. Appx105-107(2:52-3:29, 5:42-53). When VDDlogic is at least the value of the memory's minimum operating voltage, VDDlogic is provided to the memory. Otherwise, VDDmem is supplied to the memory. Appx106(3:30-44, 3:54-4:7).

VLSI asserted claims 1, 5, 6, 9, and 11. Representative claim 1 provides:

1. A method, comprising:

providing an integrated circuit with a memory;

operating the memory with an operating voltage;

determining a value of a minimum operating voltage of the memory;

providing a non-volatile memory (NVM) location;

storing the value of the minimum operating voltage of the memory in the NVM location;

providing a functional circuit on the integrated circuit exclusive of the memory;

providing a first regulated voltage to the functional circuit;

providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;

providing the first regulated voltage as the operating voltage of the memory ***when the first regulated voltage is at least the value of the minimum operating voltage***; and

providing the second regulated voltage as the operating voltage of the memory ***when the first regulated voltage is less than the value of the minimum operating voltage***, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

Appx111(13:7-28).[3]

Independent claim 9 is similar. It recites "a memory location that stores a value representative of the minimum operating voltage" of the memory, and a

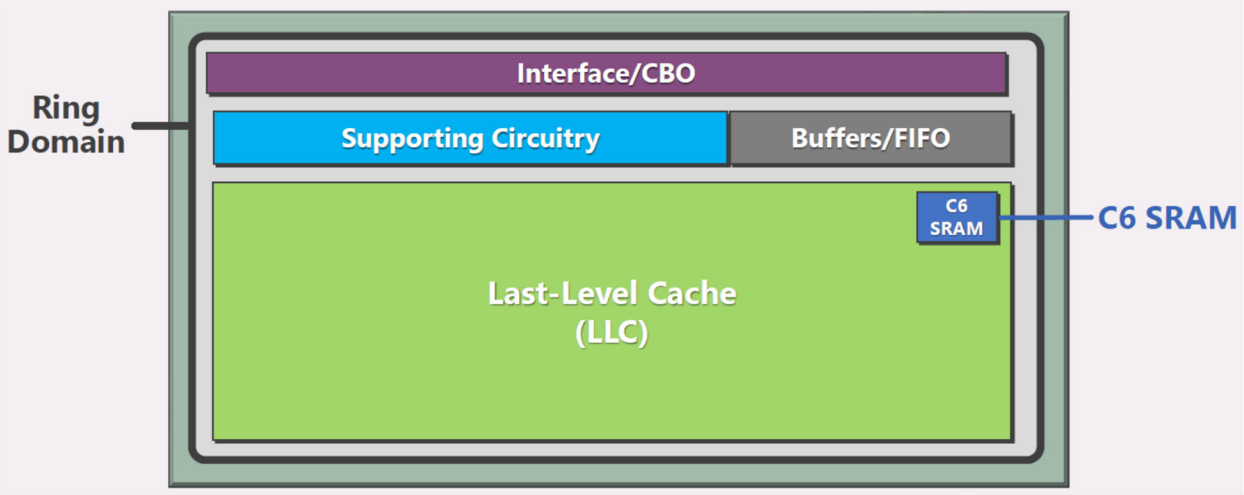
[3] Emphasis is added unless indicated otherwise.

"power supply selector" that supplies either a "first regulated voltage" or a "second regulated voltage" to the memory based on the same relationship between the first regulated voltage and the memory's minimum operating voltage as in claim 1. Appx111(13:59-14:15).

2. Intel's accused C6SRAM multiplexer

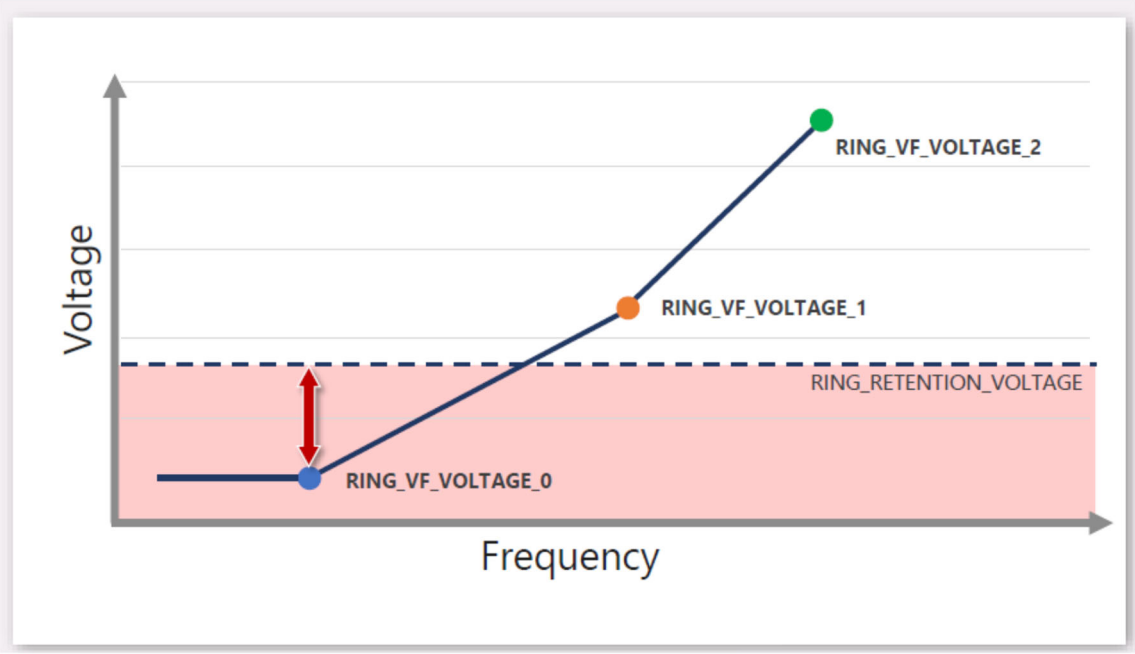
VLSI accused Intel's Haswell and Broadwell microprocessors of infringing the '373 patent. Appx1447. Each microprocessor chip includes multiple processor cores, which operate in different "states" depending on performance needs, plus various memories and other components. Appx1841-1845.

VLSI's infringement claim focused on Intel's C6SRAM. Appx1453. The C6SRAM is a small memory that, along with the last-level cache memory and other components, collectively form the "ring" domain:



Appx15344; *see* Appx1842-1845; Appx2726-2727. The C6SRAM serves one purpose: it stores processor state data when an associated processor core is turned off (or "sleeping"). Appx1395; Appx1833-1834; Appx1938.

Under most circumstances, the ring components (including the C6SRAM) receive a voltage from the "VCCR" supply. Appx1845; Appx1939. During operational states when the chip's processor cores are awake, the VCCR voltage level is set based on a value stored in one of the RING_VF_VOLTAGE_0, RING_VF_VOLTAGE_1, or RING_VF_VOLTAGE_2 fuses[4]:



Appx15343; *see* Appx1850-1855; Appx1949-1950; Appx2757-2760. During certain states when some processor cores are asleep, the VCCR voltage level is set

[4] A "fuse" stores information and does not lose its value when removed from power. Appx1853. Intel sets the fuse values in each chip during manufacturing. Appx2678.

based on the RING_RETENTION_VOLTAGE fuse value. Appx1859-1861; Appx1951. As illustrated above, RING_RETENTION_VOLTAGE is ***not*** the C6SRAM's lowest operating voltage as it is ***greater than*** RING_VF_VOLTAGE_0. Appx1860; Appx1945-1950; Appx2015-2017; Appx2742-2744; Appx15342.

Whenever the chip enters a deep sleep state called "Package C7" (i.e., when ***all*** processor cores are asleep (Appx1388)), a multiplexer switches the C6SRAM's voltage supply from VCCR to a second supply called "VCCIO" and the ring components other than the C6SRAM are essentially turned off. Appx1845-1849; Appx1862-1865; Appx1939-1940; Appx1960; Appx2669-2670. RING_RETENTION_VOLTAGE is ***not*** involved in this voltage-switching process. Appx1862; Appx2744-2747.

C. VLSI's Assertion Of The '759 Patent

1. The '759 patent

The '759 patent relates to "managing clock speeds within electronic devices." Appx120(1:6-7). Clock speed, or frequency, is the speed at which the electronic device operates. Appx1384. The '759 patent describes a technique for managing clock speed where a "first master device" (120 below) sends a "request" to a "clock controller" (150) to change the frequency of a "bus" (102) and other devices (e.g., 122) connected via the bus:

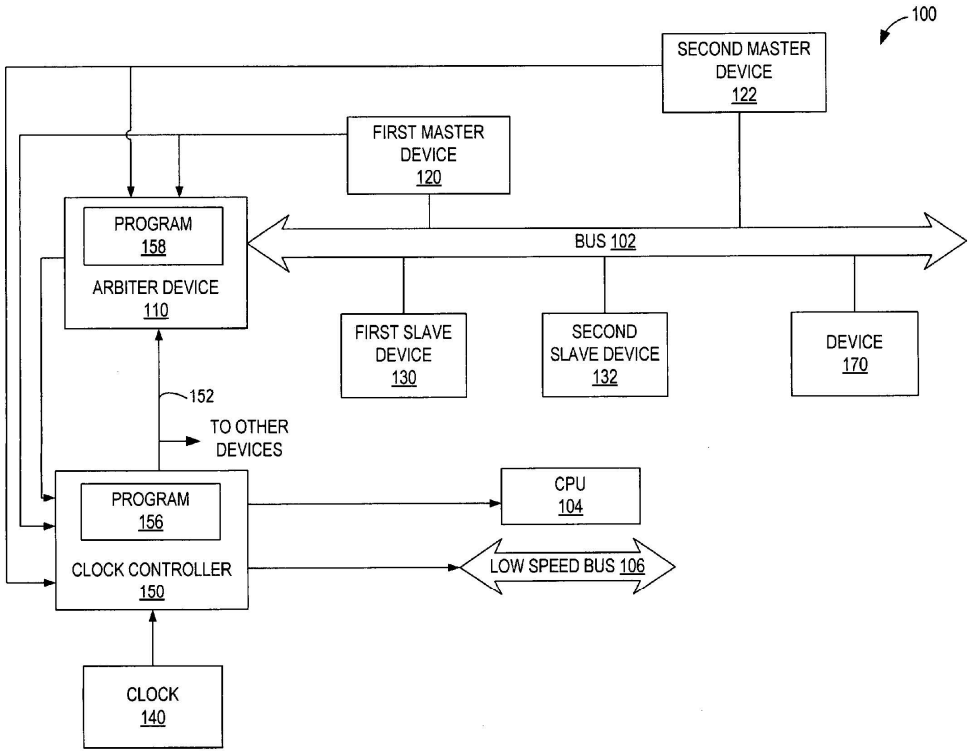


FIG. 1

Appx114.

VLSI asserted claims 14, 17, 18, and 24. Representative claim 14 provides:

14. A system comprising:

a bus capable of operation at a variable clock frequency;

a first master device coupled to the bus, ***the first master device configured to provide a request to change a clock frequency of a high-speed clock*** in response to a pre-defined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

a programmable clock controller having an embedded computer program therein, the computer program including instructions to:

receive the request provided by the first master device;

> provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device; and
>
> provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

Appx123-124(8:50-9:4). Independent claim 18 similarly recites a system where "the ***clock controller*** [is] configured to ***receive a request*** to change the clock frequency of the high-speed clock ***from the first master device***[.]" Appx124(9:19-40).

During prosecution, the applicant amended the claims eight times, including to overcome rejections based on U.S. Patent No. 7,007,121 ("Ansari"). Among those amendments, the applicant canceled claims reciting that "***at least*** one master device" provide an input "includ[ing] a request to change the variable clock frequency" (Appx8316-8317), and rewrote the claims to more narrowly require that "the master device … provide a request to change the clock frequency" (Appx8368).

2. Intel's accused SpeedShift feature

VLSI accused Intel's "Lake" microprocessors of infringing the '759 patent. Appx1462. VLSI's infringement claim focused on Intel's SpeedShift technology—a collection of sophisticated algorithms that Intel's engineers developed to autonomously manage power and performance. Appx2073-2074; Appx2179-2183. These algorithms are implemented in source code (called "p-code") running on the power control unit ("PCU"), which is a separate component from the processor cores

whose power and performance they manage. Appx2137; Appx2697; Appx2748-2751. Intel's processor cores do not send requests to change frequency based on changes in their own individual performance. Instead, the PCU decides whether to change frequency based on SpeedShift's ongoing observations of the system as a whole. Appx2083-2085; Appx2188-2189.

D. Intel's License Defense

In July 2020, Fortress—which formed and controls VLSI—acquired control of Finjan Holdings, LLC ("FHL"). Appx3009. That acquisition triggered Intel's rights under a 2012 license to practice patents owned by FHL's subsidiaries and their "Affiliates," a broadly-defined term that includes VLSI. Appx3684(§1.2). In August 2020, Intel notified VLSI and Fortress that the acquisition meant Intel had a license to VLSI's asserted patents. Appx3017-3019. Intel moved to stay the litigation in September 2020 and to amend its answer to add this license defense in November 2020. Appx3001-3015; Appx3631-3644.

E. Trial

In December 2020, over Intel's objections, the district court transferred the case from Austin to Waco for trial. Appx3841-3851. Trial was held during February/March 2021.

1. Fortress evidence

The district court initially ruled there was "no way to not allow a discussion of VLSI's relationship with Fortress" at trial because it was relevant to the jury's understanding of VLSI, assessing damages, and determining witness credibility. Appx4874. After all, Fortress created VLSI, arranged for VLSI's purchase of the patents-in-suit, holds a majority of VLSI's board seats, and would share in any recovery. Appx3975-3976; Appx3856-3857. Before opening statements, however, the court reversed course and precluded Intel from mentioning Fortress during trial. Appx3947-3951.

2. VLSI's infringement case

VLSI presented its infringement case through its expert Tom Conte. For the '373 patent, Dr. Conte testified that RING_RETENTION_VOLTAGE was ***literally*** the claimed "***minimum*** operating voltage" of Intel's C6SRAM. Appx1451; Appx2727-2728. He offered that opinion even though the C6SRAM can and does operate at a ***lower*** voltage. *Infra* pp. 27-30. Dr. Conte also contended that a multiplexer selects which voltage to provide to the C6SRAM in the claimed manner, despite admitting that the multiplexer does ***not*** actually use RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage") when making that selection. Appx2735-2736.

For the '759 patent, Dr. Conte presented a doctrine-of-equivalents theory as an alternative to literal infringement, but that theory encompassed claim scope surrendered during prosecution. Appx2704. More specifically, Dr. Conte testified that the ***combination*** of a processor core (the alleged "first master device") and p-code running on the PCU (the alleged "clock controller") provided the claimed "request" to change frequency. Appx2705-2709; Appx15183-15186. Dr. Conte did not explain how this combination operated in substantially the same way as the claimed invention. Nor could he show how his equivalents theory—where the PCU (the alleged "clock controller") sends the claimed request to itself—comports with the claim language, which requires the master device to "provide" and the clock controller to "receive" the request. *Infra* pp. 42-45.

3. Damages evidence

After denying Intel's *Daubert* challenges, the district court allowed VLSI to present its damages case through its expert Ryan Sullivan. Appx1-2. Dr. Sullivan relied on a regression model—which he created only for litigation and which included ***non-accused products and features*** (*e.g.*, Appx1713; Appx1720-1721)—to purportedly determine the relationship between frequency and price in Intel's products. Appx1611-1614. He multiplied that result by the purported power and performance benefits attributable to the patents, as determined through testing done by VLSI expert Murali Annavaram—which again included ***non-accused products***

and features (*e.g.*, Appx1555-1566). Appx1606-1607; Appx1654-1658; Appx1702-1704; Appx15290; Appx15293.[5] Dr. Sullivan applied that number to Intel's accused revenues to calculate the revenues allegedly attributable to the accused features. Appx1654-1658. He then performed a so-called "cost and contribution apportionment" step in which he subtracted Intel's spending costs from the calculated revenues and allocated the entire result—i.e., ***all*** of Intel's alleged incremental profits—to VLSI. Appx1658-1664; Appx15294. From those calculations, Dr. Sullivan concluded that a reasonable royalty would be $1.61 billion for the '373 patent and $832 million for the '759 patent. Appx1663-1664; Appx15303; Appx15305.

On the last trial day, the district court overruled Intel's objections[6] and allowed VLSI to introduce evidence of six ***noncomparable*** agreements in which Intel had paid between $200 million and $1.5 billion to settle unrelated litigation and to license hundreds of unrelated patents. Appx2328-2331; Appx2804-2808.

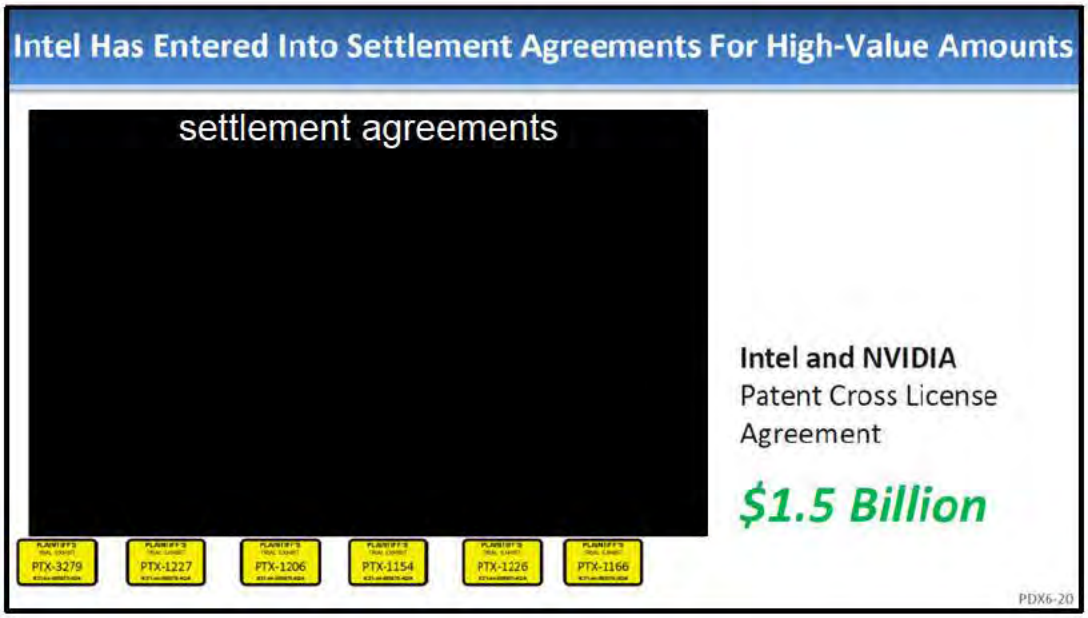
Intel subsequently called its damages expert Hance Huston. He testified that a reasonable royalty would be $2.2 million, based on prior transactions involving the asserted patents and 20 agreements that he explained were ***comparable*** to the

[5] Dr. Sullivan assumed a 1% frequency increase equaled a 1% performance or power savings increase. Appx1606-1607.

[6] Appx3570-3579; Appx3626-3629; Appx3712-3713; Appx3722-3725; Appx3903-3904; Appx3986-3987; Appx2502; Appx2799-2801; Appx2804.

hypothetical license. Appx2374; Appx2764-2784; *see* Appx2370-2381; Appx15392-15409. On cross-examination, and over Intel's continuing objection, VLSI brought up the ***noncomparable*** Intel settlements—emphasizing that "Intel has paid much more than single-digit millions to license[] patents in litigation," including "$1.5 billion to license patents from … NVIDIA[.]" Appx2800-2802.

VLSI then called its licensing expert Mark Chandler for the first time in its rebuttal case—and as the last trial witness. Mr. Chandler agreed that the six Intel settlement and cross-license agreements were ***"not comparable"*** to a hypothetical license to the asserted patents. Appx2513; Appx2516-2517; *see* Appx2807-2808. He nevertheless testified that these agreements would have been "informative" to the hypothetical negotiation (Appx2515-2516) and emphasized the "high-value" amounts Intel paid for each settlement:



Appx15236; *see* Appx2803-2806; Appx15231-15236.

4. Verdict

The next day, the jury found that Intel infringed the '373 patent literally and the '759 patent by equivalents (but not literally). Appx9-10. The jury also found that Intel had not proved the '759 patent invalid. Appx12.

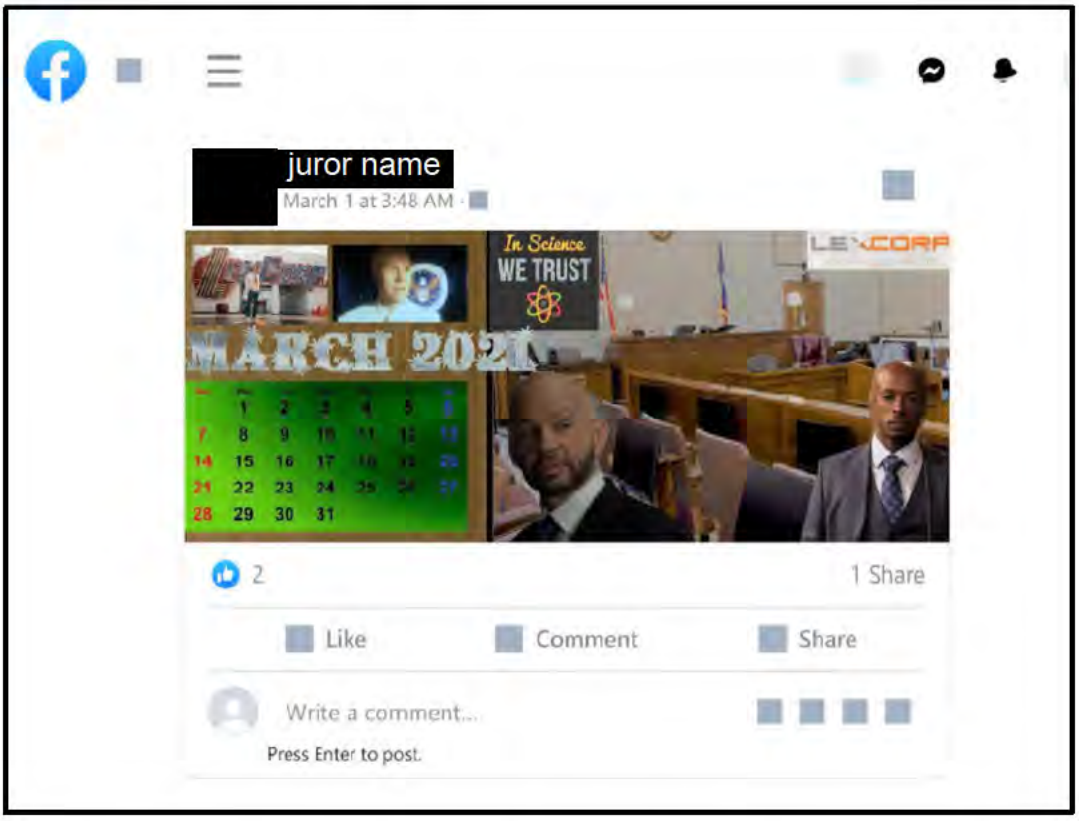
The jury awarded $1.5 billion for the '373 patent and $675 million for the '759 patent. Appx13-14. Although these amounts did not match the reasonable-royalty numbers presented by any expert, they did match what Intel paid to settle two of the unrelated litigations that VLSI told the jury about. In fact, the jury's $1.5 billion award matched a number found only one place in the record: Intel's settlement payment to NVIDIA. Appx2805. And the jury's $675 million award matched Intel's settlement payment to Intergraph as reported by the *New York Times*. Appx4047-4048. That the jury awarded this precise amount, which was not stated at trial, was either a remarkable coincidence or an indication the jury consulted extra-record material—as VLSI's counsel suggested during closing arguments and later events involving one juror confirmed had occurred. *See infra* p. 21.[7]

[7] Mr. Chandler testified that the Intergraph settlement was for settlement amount (Appx2805), but VLSI's counsel stated during closing that what Intel paid in one settlement "was published in the New York Times" (Appx2622). A simple Internet search returns the *New York Times* article and others reporting the Intergraph amount as $675 million. Appx4046-4058.

F. Post-Trial Proceedings

1. Intel's juror misconduct motion

After the verdict, Intel learned that—despite admonitions not to research or communicate about the case (Appx1182-1185; Appx2305)—a juror posted the following on Facebook ***during trial***:



Appx4040. The juror's post depicted actors who played Superman villain Lex Luthor, likening Intel to Luthor's international conglomerate "LexCorp." This was superimposed on a photograph of the Waco courtroom where trial was held—taken from the "IPWatchdog" blog. Appx4039-4045.

Intel moved for a new trial because the Facebook post showed the juror improperly communicated about the case during trial and consulted extra-record information. Appx4015-4038. In September 2021, the district court denied Intel's motion and refused to hold an evidentiary hearing to investigate the juror's misconduct and its impact on the verdict. Appx4508-4520.

2. Intel's other post-trial motions

In August 2021 and March 2022, the district court rejected Intel's requests for JMOL or a new trial on infringement, invalidity, and damages. Appx16-22; Appx74-97. The court separately ruled that prosecution history estoppel did not bar VLSI's equivalents theory for the '759 patent. Appx49-53.

3. Intel's license defense

In March 2022, the district court also denied Intel's motion to add its license defense—which Intel had filed 16 months earlier—on the grounds that Intel's motion was untimely, amendment was futile, and VLSI would be prejudiced because trial already occurred. Appx65-73.

4. Final judgment

In April 2022, the district court awarded $162 million in pre-judgment interest and entered judgment. Appx98-100; Appx4521-4527.

SUMMARY OF ARGUMENT

1. The infringement judgment for the '373 patent should be reversed. No reasonable jury could find that RING_RETENTION_VOLTAGE is ***literally*** a "***minimum*** operating voltage" of Intel's C6SRAM because the evidence established that the C6SRAM can and does operate at a ***lower*** voltage. Nor could a reasonable jury find that Intel's products use RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage") in determining "when" to provide either of two voltages to the C6SRAM as the claims require. Instead, Intel's products switch the C6SRAM's voltage supply whenever the chip enters the Package C7 sleep state—without consideration of RING_RETENTION_VOLTAGE.

2. The infringement judgment for the '759 patent should likewise be reversed. Prosecution history estoppel bars the jury's equivalents finding because, to overcome prior-art rejections, the applicant narrowed the claims by amending them to require that "the master device" (rather than "the ***at least*** one master device") provide the request to change frequency, and VLSI's equivalents theory improperly sought to recapture the surrendered claim scope. Additionally, substantial evidence does not support the jury's infringement finding because Dr. Conte offered only conclusory testimony on equivalents, and his nonsensical theory—where the PCU (the alleged "clock controller") ***both*** sends and receives the request to change frequency—is incompatible with the claim language, which requires the master

device to "provide" the request and the clock controller to "receive the request provided by the first master device."

3. A new trial is required because the district court erroneously and prejudicially allowed VLSI to introduce six agreements where Intel had paid between $200 million and $1.5 billion to settle unrelated litigation and to license hundreds of unrelated patents. VLSI's own licensing expert admitted that these agreements were ***not comparable*** to a hypothetical license to the asserted patents. And contrary to the district court's post-trial rationalization, VLSI's last-minute introduction of these noncomparable agreements was not "proper rebuttal" to Intel's damages expert, who presented a traditional reasonable-royalty analysis based on prior transactions involving the asserted patents and several ***comparable*** agreements. VLSI unfairly used the noncomparable agreements to portray Intel as a serial infringer who pays large amounts to license patents in litigation, which inflated the jury's damages analysis and tainted the entire verdict.

4. A new trial is also warranted because VLSI's damages theory should have been excluded and cannot support the jury's award. VLSI was required "to seek only those damages attributable to the infringing features." *VirnetX, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1326 (Fed. Cir. 2014). Yet VLSI's damages expert applied a regression analysis that included ***non-accused products and features***, while failing to include the accused features, and relied on technical inputs regarding

the patented features' purported benefits that were similarly derived using ***non-accused products and features***. He then allocated ***all*** of Intel's incremental profits to VLSI, though such disgorgement of profits was neither a viable legal remedy nor factually supported. Finally, VLSI's expert prejudicially compared the revenues he attributed to the asserted patents with Intel's ***total accused revenues*** in violation of the entire market value rule.

5. The district court abused its discretion by not allowing Intel to add a license defense that arose during the litigation. As a result of a prior license agreement, Intel became licensed to the '373 and '759 patents when Fortress—which formed and controls VLSI—acquired a Finjan entity in July 2020. Intel's amendment was timely, as Intel promptly notified VLSI and the court about its license defense and moved to amend its answer while following the dispute resolution procedures required by the license itself. Intel's amendment was not futile because the license's plain language—under which VLSI is an "Affiliate" due to Fortress's control of VLSI—makes clear that the license applies here.

ARGUMENT

I. STANDARD OF REVIEW

The Fifth Circuit reviews the denial of JMOL *de novo*. *ACCO Brands, Inc. v. ABA Locks Mfrs. Co.*, 501 F.3d 1307, 1311-1312 (Fed. Cir. 2007). Evidentiary rulings and rulings on motions to amend pleadings are reviewed for abuse of

discretion. *Knight v. Kirby Inland Marine Inc.*, 482 F.3d 347, 351 (5th Cir. 2007); *Meaux Surface Protection, Inc. v. Fogleman*, 607 F.3d 161, 167 (5th Cir. 2010). An "erroneous view of the law" is "necessarily" an abuse of discretion. *Highmark Inc. v. Allcare Health Mgmt. Sys., Inc.*, 572 U.S. 559, 563 n.2 (2014).

Infringement and damages are reviewed for substantial evidence following a jury verdict. *Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1309-1310 (Fed. Cir. 2009). Whether prosecution history estoppel applies is reviewed *de novo*. *Pharma Tech Solutions, Inc. v. LifeScan, Inc.*, 942 F.3d 1372, 1380 (Fed. Cir. 2019). Factual findings made by the court are reviewed for clear error. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 493 F.3d 1368, 1376 (Fed. Cir. 2007).

II. THE INFRINGEMENT JUDGMENT FOR THE '373 PATENT SHOULD BE REVERSED.

The jury found ***literal*** infringement of the '373 patent. Appx9.[8] However, there was no substantial evidence that Intel's products store or use a "minimum operating voltage" of the C6SRAM as the claims require.

A. Intel's Products Do Not Store The Claimed "Minimum Operating Voltage."

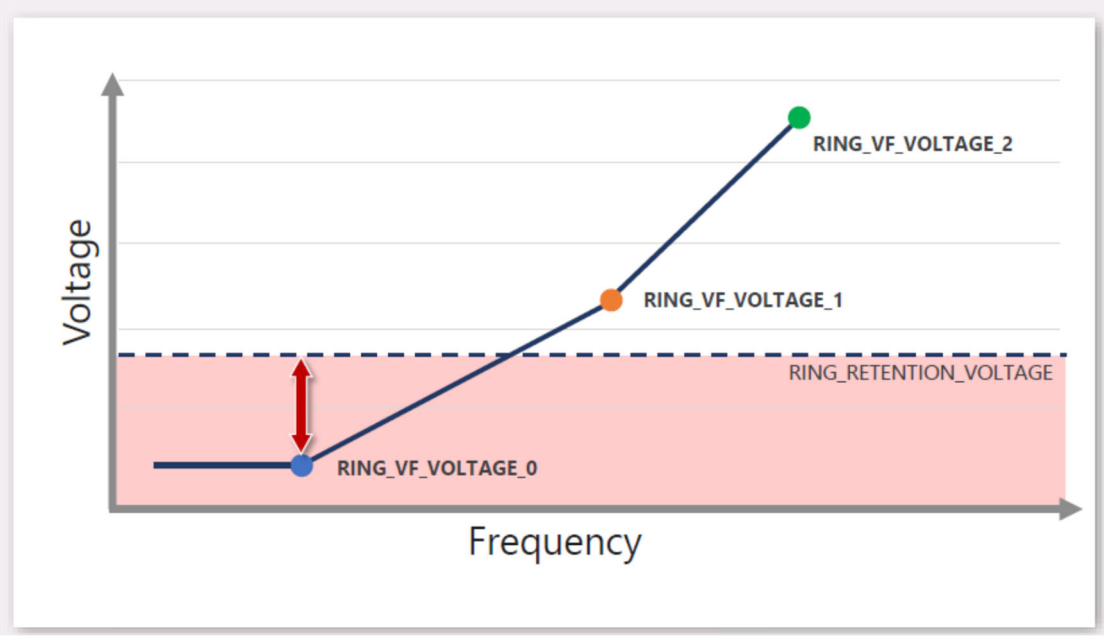
Each asserted claim requires storing "the value of the minimum operating voltage of the memory" or "a value representative of the [memory's] minimum

[8] VLSI abandoned its doctrine-of-equivalents assertion for this patent at trial. Appx1451; *see* Appx3807-3808.

operating voltage." Appx111(13:13-14, 13:63-64). VLSI identified Intel's C6SRAM as the accused "memory" and the RING_RETENTION_VOLTAGE fuse value as the accused "minimum operating voltage." Appx1403-1404; Appx2661-2662; Appx15091; Appx15097.

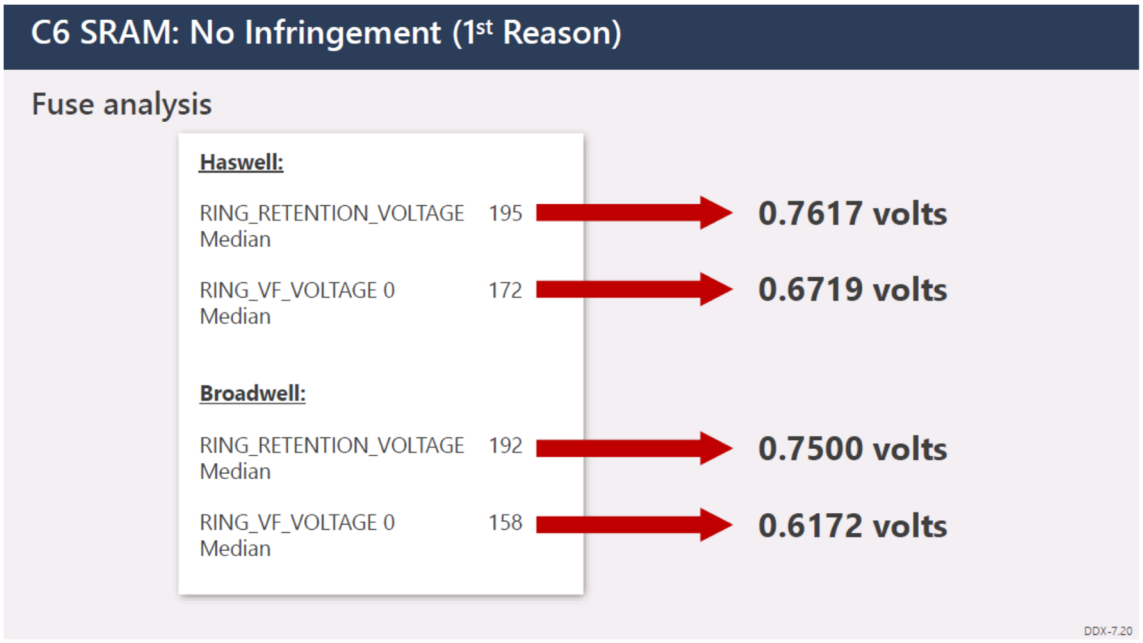
VLSI's expert Dr. Conte testified that RING_RETENTION_VOLTAGE is the "minimum retention voltage" of the C6SRAM, and he identified no other supposed "minimum operating voltage." Appx2727-2728; *see* Appx2656-2657; Appx2661; Appx2725; Appx2730-2731. Dr. Conte agreed that a "minimum retention voltage" is "the ***minimum*** voltage required to hold data." Appx2730; Appx2730-2731 ("minimum" means "the ***lowest*** value"). "In other words," Dr. Conte explained, "you['ve] got to keep power on the memory and you['ve] got to keep ***above*** this" minimum value. Appx1403.

But Intel's RING_RETENTION_VOLTAGE is merely ***a*** voltage at which the C6SRAM ***can*** retain data, not the ***"minimum"*** voltage at which data retention occurs. As Intel's engineers explained, the C6SRAM is "fully operational" and retains data at a RING_VF_VOLTAGE_0 voltage that is ***lower*** than RING_RETENTION_VOLTAGE:



Appx15343; Appx15322; Appx1854-1855; *see* Appx1859-1861 ("Q. From a voltage perspective, is RING_RETENTION_VOLTAGE level higher or lower than Ring_VF_Voltage_0? A. The voltage level is higher."); Appx2757-2760; Appx14252-14280.

Intel's expert Dennis Sylvester confirmed this fact by analyzing fuse data taken from the actual accused products. He explained that the RING_VF_VOLTAGE_0 values (which have a median value of 0.6719 volts in Haswell and 0.6172 volts in Broadwell across millions of individual chips) are ***"significantly lower"*** than the RING_RETENTION_VOLTAGE values (which have a median value of 0.7617 volts in Haswell and 0.7500 volts in Broadwell):



Appx15342; Appx1945-1950; *see* Appx2015 ("Ring_VF_Voltage_0 was significantly below [0.75 volts] in the data I actually collected from the products."); Appx2015-2017; Appx2742-2744; Appx14224-14251.

VLSI's expert Dr. Conte agreed that RING_RETENTION_VOLTAGE is set to about 0.75 or 0.76 volts in Intel's products. Appx2731. Yet he admitted on cross-examination that, when he conducted his infringement analysis, he did not investigate whether the C6SRAM ever operates at voltages ***below*** that RING_RETENTION_VOLTAGE. Appx2732. And when confronted with Intel's evidence about RING_VF_VOLTAGE_0, Dr. Conte agreed "[i]t's a ***voltage*** that's actually used" in Intel's products. Appx2436-2437. Given this evidence, no reasonable jury could find that RING_RETENTION_VOLTAGE—which is ***greater***

than RING_VF_VOLTAGE_0—is ***literally*** the "***minimum*** retention voltage" (or any other "***minimum*** operating voltage") of the C6SRAM.

The district court nonetheless denied JMOL, relying primarily on Dr. Conte's testimony claiming that Intel's witnesses failed to account for "inverse temperature dependence" (voltage adjustments based on temperature) and his unsupported conclusion that, when those adjustments are made, the operating ***voltage*** derived from the RING_VF_VOLTAGE_0 fuse value is always greater than RING_RETENTION_VOLTAGE. Appx78 (citing Appx2425-2432; Appx2434-2437; Appx2450-2452). But Dr. Conte never explained what those supposed RING_VF_VOLTAGE_0 voltages were and never performed any calculations to show how Intel's RING_VF_VOLTAGE_0 voltages supposedly should have been adjusted. The ***only voltages*** for RING_VF_VOLTAGE_0 presented to the jury were from Intel's expert's analysis of the fuse data taken from the accused products, and it is ***undisputed*** that those voltages were "significantly lower" than RING_RETENTION_VOLTAGE. *Supra* pp. 27-30.

Ignoring that Dr. Conte never identified any RING_VF_VOLTAGE_0 voltages used in Intel's products, the district court found that Dr. Conte's ultimate conclusion was "corroborated" by a few pages from Intel's documents. Appx78. It was not. None of the documents cited by the court (or otherwise relied on by VLSI) specified the voltages for RING_VF_VOLTAGE_0 in Intel's products, much less

showed that they are always greater than RING_RETENTION_VOLTAGE as Dr. Conte contended.

For example, the district court referenced a draft Intel specification showing a "Vretention" line below a "v/f 0" point on a graph and Dr. Conte's unsupported say-so that this "Vretention" was RING_RETENTION_VOLTAGE. Appx14103; Appx2425-2426. This document, however, describes a generic voltage at which data retention occurs ("Vretention"). Appx14103; Appx2017 ("That's just a line saying that you should be able to retain down below there."). It says nothing about the RING_RETENTION_VOLTAGE at the center of VLSI's infringement theory. Appx14103; Appx2016-2018. And this draft specification, which Dr. Conte agreed was "not a final description of the products" (Appx2435-2436), nowhere identifies the actual fuse settings or voltages implemented in Intel's products.

VLSI also relied on an Intel spreadsheet using the term "Vmin." Appx11359-11362. But Intel's expert—the only witness who discussed this document at trial—explained that this "Vmin" refers to an "active voltage[] to meet performance specifications," not to any minimum operating voltage or minimum retention voltage, and has nothing to do with RING_RETENTION_VOLTAGE. Appx2013-2015.

The district court further pointed to two Intel specifications stating that "RING_RETENTION_VOLTAGE … defines the worst case retention voltage ***for***

RING." Appx9574; Appx12642; *see* Appx2656-2657. But, again, these documents do not identify any fuse values or voltages used in Intel's products. And as Dr. Conte admitted, these specifications indicate that RING_RETENTION_VOLTAGE applies not just to the C6SRAM, but to the ***entire ring domain*** which also includes the last-level cache memory. Appx2725-2728. The district court dismissed this distinction, stating that the patent does not "require that the RING_RETENTION_VOLTAGE apply to the C6 SRAM specifically." Appx79. But the claims require storing "the minimum operating voltage ***of the memory***" (Appx111(13:13-14); *see id.*(13:63-64)), and VLSI identified only the C6SRAM as the accused "memory" (Appx1403). VLSI was therefore required to prove that RING_RETENTION_VOLTAGE is a "minimum operating voltage" ***of the C6SRAM***, not of some larger collection of components containing the C6SRAM.[9]

Ultimately, Dr. Conte's hand-waving analysis cannot change the fact that the ***only voltages*** for RING_VF_VOLTAGE_0 in Intel's products presented to the jury were undisputedly ***lower*** than RING_RETENTION_VOLTAGE. The evidence thus supports only one conclusion: RING_RETENTION_VOLTAGE is not ***literally*** a "***minimum*** operating voltage" of the C6SRAM. Dr. Conte's unsupported opinion

[9] The district court further stated that Dr. Conte's testimony was "corroborated" by source code. Appx77-78. But Dr. Conte simply said he reviewed Intel's code; he did not identify any code supporting his conclusions for this limitation. Appx2451-2452; Appx1380-1382; Appx1404.

to the contrary cannot sustain the infringement verdict. *Wisconsin Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1350 (Fed. Cir. 2018) (despite Dr. Conte's contrary expert conclusion, finding "insufficient evidence to support the jury's finding that [the accused] products literally satisfy the [disputed] limitation"); *Guile v. United States*, 422 F.3d 221, 227 (5th Cir. 2005) ("'A claim cannot stand or fall on the mere *ipse dixit* of a credentialed witness.'").

B. Intel's Products Do Not Provide The First And Second Regulated Voltages "When" The Claims Require.

Each asserted claim additionally requires using the memory's "minimum operating voltage" in determining which of two voltages to supply to the memory. Specifically, the claims require providing "as the operating voltage of the memory" (1) "the first regulated voltage … ***when the first regulated voltage is at least … the minimum operating voltage***," and (2) "the second regulated voltage … ***when the first regulated voltage is less than [or below] … the minimum operating voltage***." Appx111(13:20-27, 14:8-13). As Dr. Conte acknowledged, these limitations "tell[] you when to use a different voltage" and both "refer to the minimum operating voltage." Appx2733-2734.

Even under VLSI's (incorrect) theory that RING_RETENTION_VOLTAGE is a "minimum operating voltage" of the C6SRAM, VLSI introduced no evidence that Intel's products ever use RING_RETENTION_VOLTAGE in determining "when" to provide each of the two regulated voltages as the claims require. In

presenting his infringement opinion for these limitations, Dr. Conte testified that a multiplexer selects between two voltages to supply to the C6SRAM: (1) VCCR, which he called the "first regulated voltage"; and (2) VCCIO, which he called the "second regulated voltage." Appx2664-2667; *see* Appx2658-2662. But as Dr. Conte admitted, he never even "mention[ed] the RING_RETENTION_VOLTAGE" when discussing "how the power mu[ltiplexer] actually operates." Appx2735-2736.

The reason for this omission is clear: RING_RETENTION_VOLTAGE plays ***no role*** in the accused voltage-switching functionality. Instead, Intel's multiplexer switches the C6SRAM's voltage supply from VCCR to VCCIO whenever the chip enters the "Package C7" sleep state. Appx1861-1862 (Intel engineer explaining "[t]here's no relationship" between RING_RETENTION_VOLTAGE and C6SRAM multiplexer function); Appx1958, Appx2744-2748 (Intel expert showing source code for this voltage-switching function does not mention RING_RETENTION_VOLTAGE); Appx14187-14209, Appx14210-14223 (source code). Even Dr. Conte ***agreed*** that Intel's source code causes the multiplexer to switch from VCCR to VCCIO whenever the chip "goes into the [Package] C7, this deep sleep." Appx2669-2670 (describing "package C-State RING_C7_entry sequence" in source code and identifying "wire that switches the mu[ltiplexer] when it goes into the package C7").

In denying JMOL, the district court stated that "Dr. Conte demonstrated that RING_RETENTION_VOLTAGE acts as the ***threshold*** for when the voltages are supplied." Appx80-81. However, Dr. Conte merely described examples where either VCCR or VCCIO is supplied to the C6SRAM based on the chip's sleep state. Appx1485; Appx2665-2668; Appx15073; Appx15076. He never showed that RING_RETENTION_VOLTAGE is actually used as a "threshold" for determining when VCCR and VCCIO are supplied—because that is not how Intel's products work.

Moreover, the district court and Dr. Conte ignored other examples confirming that Intel's products do the ***opposite*** of what the "when" limitations require. For instance, VCCR (the alleged "first regulated voltage") is supplied to the C6SRAM at times when it is ***below*** RING_RETENTION_VOLTAGE (i.e., when VCCR is at RING_VF_VOLTAGE_0). *Supra* pp. 27-30. And VCCIO (the accused "second regulated voltage") is supplied to the C6SRAM at times when VCCR is still ***at or above*** RING_RETENTION_VOLTAGE. Appx1862-1863 (Intel engineer explaining that multiplexer switches from VCCR to VCCIO ***before*** turning VCCR supply off). These examples conclusively demonstrate that Intel's products do not operate as the "when" limitations require.

The district court tried to downplay Dr. Conte's admission that "he did not refer to RING_RETENTION_VOLTAGE in describing multiplexer operation" as

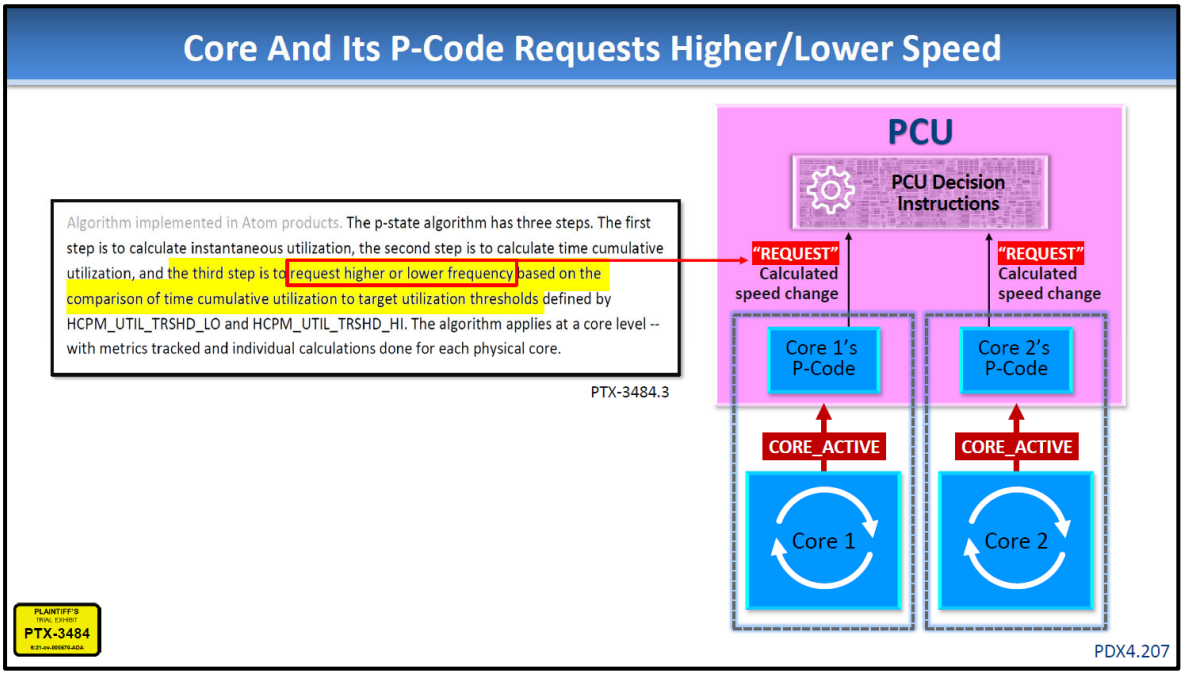
"merely introduc[ing] a factual dispute." Appx81; *see* Appx2735-2736. On the contrary, Dr. Conte's admission makes clear there was no factual dispute on this point—all witnesses ***agreed*** that Intel's products do not actually use RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage") in determining "when" to supply which voltage to the C6SRAM. *Supra* p. 34. Yet that is exactly what the plain claim language requires. *Supra* pp. 7-10, 33.

The district court further stated that Dr. Conte "supported his testimony with Intel documents," although it identified no such documents. Appx81. In fact, Intel's documents show that Intel's multiplexer switches the C6SRAM's power supply from VCCR to VCCIO whenever the chip enters the Package C7 sleep state. Appx8830-8831 (Intel specification stating that multiplexer switches when "Vccr is powered down" (i.e., when the chip enters Package C7)); Appx14187-14209, Appx14210-14223 (source code describing Package C7 entry sequence). None of these documents mentions RING_RETENTION_VOLTAGE, much less suggests that Intel's multiplexer somehow uses that value in determining "when" to supply VCCR or VCCIO to the C6SRAM.

For these reasons, no reasonable jury could find that Intel's products ***literally*** satisfy the "when" limitations.

III. THE INFRINGEMENT JUDGMENT FOR THE '759 PATENT SHOULD BE REVERSED.

Each asserted claim of the '759 patent requires: (1) a "first master device" that "provide[s]" or "sen[ds]" a "request" to change frequency; and (2) a "clock controller" that "receive[s] the request provided by the first master device[.]" Appx123-124(8:50-9:4, 9:19-40). VLSI's expert Dr. Conte presented an equivalents theory accusing the ***combination*** of a processor core (the alleged "first master device") and p-code running on the PCU (the alleged "clock controller") of providing the claimed "request" in Intel's products:



Appx15183; *see* Appx2707-2709 ("The claim says 'the first master device provides a request.' Now, it's the first master device ***and*** its P-code that provides the request."); Appx2708 (testifying that p-code "is running in the PCU"). VLSI's

equivalents theory—which the jury adopted (Appx10)—is barred by prosecution history estoppel and unsupported by substantial evidence.[10]

A. Prosecution History Estoppel Bars VLSI's Equivalents Theory.

During prosecution, the applicant amended the '759 patent claims to overcome repeated rejections based on the Ansari reference. The proposed claims originally recited that "***at least*** one master device" provides a trigger input that includes a "request" to change frequency, and thus allowed multiple components to trigger the request. Appx8044-8045; Appx8237-8238; Appx8273-8274; Appx8316-8317. In four consecutive rejections, the examiner found that Ansari disclosed this "request" limitation and cited functionality performed by two components in Ansari (a master device and an arbiter). Appx8205 (explaining that, in Ansari, the "***[a]rbiter changes the frequency*** based on size of transaction," which "is part of trigger input from ***master*** to ***arbiter*** to ***change the frequency***"); Appx8257; Appx8305-8306; Appx8349; *see* Appx8263; Appx8298-8302; Appx8338-8340; Appx8343-8345; Appx4478-4496.

In response, the applicant attempted to distinguish Ansari by asserting that "[t]he master device does not determine or request a desired bus frequency because ***it is the bus arbiter*** that determines the bus frequency[.]" Appx8242-8243;

[10] For his literal-infringement theory, Dr. Conte alleged that the core alone sends the claimed "request." Appx2691-2695; Appx15153. The jury correctly rejected that theory. Appx9.

Appx8277-8278; Appx8319; Appx8325. After these efforts failed, the applicant canceled all pending claims and rewrote the "request" limitations as demonstrated by the following representative comparison:

Pre-Amendment Claim 22	Post-Amendment Claim 44
at least one master device coupled to the bus, … wherein ***the at least one master device*** provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency	***a master device*** coupled to the bus, ***the master device*** … provide[s] a request to change the clock frequency … in response to a predefined change in performance of ***the master device***

Appx8316-8317; Appx8368; *see* Appx50. Only ***after*** the applicant narrowed the claims to require that "the master device" (rather than "the ***at least*** one master device") provide the "request" to change frequency did the examiner withdraw the Ansari-based rejections. Appx8392-8394; Appx8432-8435; Appx8472.

Prosecution history estoppel bars VLSI's attempt to reclaim through equivalents what the applicant surrendered during prosecution. The amendment described above was made for a substantial reason of patentability—namely, to overcome prior-art rejections. *Pioneer Magnetics, Inc. v. Micro Linear Corp.*, 330 F.3d 1352, 1357 (Fed. Cir. 2003). And it was narrowing because the applicant canceled claims that allowed the first master device in combination with other components ("the ***at least*** one master device") to provide the request to change frequency, and replaced them with claims requiring "the master device" to provide that request. *Supra* pp. 38-39. This narrowing amendment is "presumed" to

disclaim "the territory between the original claim and the amended claim." *Pharma Tech*, 942 F.3d at 1380. VLSI is therefore barred from relying on Dr. Conte's equivalents theory, which alleged that the master device in combination with another component (the PCU) provided the claimed "request." Appx2707-2709.

VLSI cannot rebut the presumption that estoppel applies. First, the alleged equivalent—the master device in combination with another component providing the request to change frequency—was foreseeable because it was disclosed in Ansari and contemplated in the rejected claim language. Second, "an amendment made to avoid prior art that contains the equivalent in question is not tangential[.]" *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 344 F.3d 1359, 1369 (Fed. Cir. 2003) (en banc). Third, there is "no other reason," such as "the shortcomings of language," that "'the [applicant] could not reasonably be expected to have described'" the alleged equivalent. *Id.* at 1370.

The district court refused to apply prosecution history estoppel ***solely*** because it concluded that the amendment described above "did not narrow the claim scope." Appx53; *see* Appx1. That conclusion was wrong, and based on clearly-erroneous factual findings. *See* Appx27-35. The amendment was plainly narrowing because the claims originally allowed multiple components working together to provide the "request," but as amended required "the master device" to do so. *Supra* pp. 38-39; *see Deering Precision Instruments, L.L.C. v. Vector Distrib. Sys., Inc.*, 347 F.3d

1314, 1325-1326 (Fed. Cir. 2003) (applying estoppel where applicant deleted original claims and added other claims with new limitation). And this amendment led the examiner to withdraw the previous Ansari-based rejections, confirming that it was narrowing. *See Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1348 (Fed. Cir. 1998) ("[I]t is difficult to conceive of many situations in which the scope of a rejected claim that became allowable when amended is not substantively changed by the amendment[.]").

The district court nonetheless reasoned that the amendment "did not impact the claim scope" because the amended claims recited "***a master device*** coupled to the bus, the master device operable to provide a request to change the clock frequency" (Appx8368) and "the indefinite article 'a' means 'at least one.'" Appx52 (citing *Crystal Semiconductor Corp. v. TriTech Microelectronics Int'l, Inc.*, 246 F.3d 1336, 1347 (Fed. Cir. 2001)). The court further stated that "[w]ithout any reference to 'alone' in any of the claims," it would "not reinterpret the Federal Circuit's instruction that 'a' means 'at least one.'" Appx52-53.

This Court does not apply such a formalistic approach devoid of context. While "[a]s a general rule, the words 'a' or 'an' in a patent claim carry the meaning of 'one or more,'" "[t]he general rule does ***not*** apply when the context clearly evidences that the usage is limited to the singular." *TiVo, Inc. v. EchoStar Commc'ns Corp.*, 516 F.3d 1290, 1303-1305 (Fed. Cir. 2008). That is the case here: the

amended claim language and prosecution history make clear that "the master device" itself—and not in combination with other components—must provide the claimed "request." *Supra* pp. 38-39; *see, e.g.*, *TiVo*, 516 F.3d at 1303-1305 ("[T]he claims and written description … make clear that the ***singular*** meaning applies" to term "***an*** MPEG stream[.]"); *Philips Elecs. N. Am. Corp. v. Contec Corp.*, 177 F. App'x 981, 987 (Fed. Cir. 2006) (construing "an entry initiate key" to mean "one entry initiate key" where "claim language was amended from '***ones*** of said keys' to '***one*** of said keys'"). Indeed, had the applicant intended the new claim language reciting "a master device" merely to cover the same scope as the original "at least one master device" language, there would have been no need to amend this language at all.[11]

Given the narrowing amendment made to the "request" limitations, prosecution history estoppel bars VLSI's equivalents theory, which improperly sought to recapture what the applicant surrendered.

B. The Jury's Infringement Finding Is Unsupported By Substantial Evidence.

To prove infringement by equivalents, VLSI had to present "'particularized testimony and linking argument' as to the insubstantiality of the differences between

[11] The district court's reference to an "informality" relates to a ***later*** amendment fixing a "lack[] [of] antecedent basis" by changing one remaining instance of "the at least one master device" to "the master device." Appx53; *see* Appx8385; Appx8405. This later amendment merely conformed language to the earlier amendment; that the examiner described the later amendment as an "informality" does not change the impact of the earlier narrowing amendment.

the claimed invention and the accused device[.]" *Akzo Nobel Coatings, Inc. v. Dow Chem. Co.*, 811 F.3d 1334, 1342 (Fed. Cir. 2016). But Dr. Conte offered only conclusory testimony on equivalents. He stated that "[t]he claim says 'the first master device provides a request'" and, under his equivalents theory, "the first master device and its P-code [on the PCU] … provide[] the request." Appx2707; *see* Appx2704-2705; Appx2707-2710. He described this alleged equivalent as a ***different*** "design choice" from what the claims recite—and nowhere explained why that difference was insubstantial or how the accused equivalent operates in substantially the same "way" as the claimed invention. Appx2707 (describing it as a "design choice" with a "***difference*** of where an engineer draws this data line"). This is legally insufficient. *Akzo*, 811 F.3d at 1342-1343 (affirming noninfringement summary judgment where "scant" equivalents discussion "fail[ed] to articulate how [the] accused process operates in substantially the same way" or "how the differences … are insubstantial"); *Augme Techs., Inc. v. Yahoo! Inc.*, 755 F.3d 1326, 1336 (Fed. Cir. 2014) (similar).

Dr. Conte's equivalents theory was also nonsensical and incompatible with the claim language. The claims require: (1) "the first master device" to "provide" a "request" to change frequency; and (2) the "clock controller" to "receive the request provided by the master device." Appx123-124(8:50-9:4, 9:19-40). Yet under Dr. Conte's equivalents theory, the ***same*** component—the PCU, which is the alleged

"clock controller" (Appx2707-2709; Appx2696-2699)—both "provides" and "receives" the request. Given this inconsistency with the claim language, no reasonable jury could find infringement. *Sage Prods., Inc. v. Devon Indus., Inc.*, 126 F.3d 1420, 1425-1426 (Fed. Cir. 1997) (when "issued patent contains clear structural limitations, … court will not effectively remove such a limitation" through equivalents); *Searfoss v. Pioneer Consol. Corp.*, 374 F.3d 1142, 1150-1151 (Fed. Cir. 2004) (no reasonable jury could find alleged equivalent—a combination of components—operated in substantially same way as claim requiring "direct connection" between components); *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1255 (Fed. Cir. 2010) (assertion that spring means and hinged arm "can be the same structure renders the asserted claims nonsensical").

The district court relied on Dr. Conte's testimony to deny JMOL, stating that "Dr. Conte distinguished the core and PCU when he testified that 'the core and Core 1's P-Code' and 'PCU decision instructions' provided and received the request, respectively." Appx87. This misses the point. The issue is not whether the core and PCU are distinct in Intel's products, but whether—contrary to the claim language—the same component is used to send and receive the request. It was undisputed that, under Dr. Conte's equivalents theory, the PCU ***both*** sends and receives the request. Appx85 (court describing Dr. Conte's equivalents theory as "the combination of core 1 ('first master device') and core 1's associated code in the

PCU ('programmable clock controller') provid[ing] the claimed 'request'"); *e.g.*, Appx2451 (Dr. Conte testifying that p-code "run[s] on … the programmable clock controller that includes the PCU"); Appx2697; Appx2706-2709 ("[Q.] [W]hat module receives this request[?] A. The PCU."); *supra* p. 37. That is what cannot satisfy the claim language.[12]

Finally, the district court abused its discretion in finding Intel waived this argument. Appx87. The court viewed Intel as "propos[ing] a new claim construction, which it waived by omission" and by "neglecting to raise the issue … in its Rule 50(a) motion." *Id.* But Intel's argument is not based on claim construction. Rather, Intel has consistently relied on the claim language's plain meaning to assert that "VLSI's argument that the 'request' limitation is satisfied by … equivalents is both factually unsupported and legally impermissible." Appx3891-3892; *see* Appx4082-4083; Appx4472-4473. And Intel's Rule 50(a) motions expressly argued that Dr. Conte's testimony "would not allow any reasonable jury to find infringement [by] equivalents" with respect to the "request"

[12] The district court cited two cases finding equivalence where the accused device used multiple components to perform functions claimed by a single component. Appx87 (citing *Intel Corp. v. ITC*, 946 F.2d 821, 832 (Fed. Cir. 1991); *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 149 F.3d 1309, 1320 (Fed. Cir. 1998)). Those cases do not hold that the same component can perform separate functions that, as here, the claims require be performed by different components interacting with each other in a specified manner.

limitations. Appx3891-3893; Appx4000-4002; *see Western Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1367-1368 (Fed. Cir. 2010) (reversing district court and finding no waiver under applicable "liberal standard").

IV. THE DISTRICT COURT ERRONEOUSLY AND PREJUDICIALLY ALLOWED VLSI TO INTRODUCE *NONCOMPARABLE* AGREEMENTS.

Over Intel's repeated objections (*supra* note 6), the district court allowed VLSI to introduce six Intel settlement and cross-licensing agreements that covered hundreds of patents unrelated to the patents-in-suit and required Intel to pay amounts ranging from $200 million to $1.5 billion.[13] There was no dispute that these agreements were ***not comparable*** to a hypothetical license to the asserted patents. The district court abused its discretion and legally erred by admitting testimony and evidence concerning these agreements, which VLSI used to tell the jury about irrelevant, high-dollar amounts paid by Intel to settle unrelated litigation. The erroneous admission of this highly-prejudicial evidence warrants a new trial.

A. VLSI's Expert Agreed The Intel Agreements Were *Not* Comparable To The Hypothetical License.

No expert offered any opinion that the six Intel agreements relied on by VLSI were comparable to a hypothetical license to the asserted patents. On the contrary, VLSI's licensing expert Mark Chandler admitted that these agreements were ***"not***

[13] The Intel agreements were with NVIDIA, Intergraph, MicroUnity, company name company name, Transmeta, and company name. Appx8645-8791; Appx8850-8872.

comparable." Appx2513; *see* Appx2516-2517 ("Q. You concluded that not a single [agreement] was comparable, right? A. Yes."). Mr. Chandler instead testified that the agreements would have been "informative" to the hypothetical negotiation. Appx2803-2804; Appx2515-2516. But he conceded that "informative" does not mean "comparable." Appx2513 (describing these agreements as "[i]nformative but not comparable").

Whether a prior agreement might be "informative" (as Mr. Chandler asserted) is legally irrelevant unless the agreement is economically and technologically comparable to the hypothetical license—which Mr. Chandler admitted was not the case here. *Elbit Sys. Land & C4I Ltd. v. Hughes Network Sys., LLC*, 927 F.3d 1292, 1299 (Fed. Cir. 2019) ("Use of actual past licenses and negotiations ***to inform the hypothetical negotiation***" requires "the prior licenses or settlements … to be 'sufficiently ***comparable***' for evidentiary purposes[.]"). For that reason alone, the noncomparable agreements should have been excluded. *Apple Inc. v. Wi-LAN Inc.*, 25 F.4th 960, 972 n.5 (Fed. Cir. 2022) ("Sufficient comparability is a threshold requirement for licenses to be admissible."); *LaserDynamics, Inc. v. Quanta Computer, Inc.*, 694 F.3d 51, 81 (Fed. Cir. 2012) (expert's use of noncomparable license rendered opinion "arbitrary and speculative").

Even worse, Mr. Chandler repeatedly emphasized that Intel paid "hundreds of millions of dollars, even billions" pursuant to the noncomparable agreements.

Appx2501; *see* Appx2516; Appx2803-2806; Appx15231-15236. Yet he nowhere accounted for the fact that the Intel agreements included "hundreds if not over 1,000 patents" (Appx2807-2808), involved different patents and technologies from the patents-in-suit, and included litigation settlements and cross-licenses. Simply put, the noncomparable agreements could not have helped the jury reliably assess damages. *Wi-LAN*, 25 F.4th at 973-974 (expert's testimony "should have been excluded" where license analysis "fail[ed] to address [how] other patents contributed to the royalty rate"); *MLC Intellectual Prop., LLC v. Micron Tech., Inc.*, 10 F.4th 1358, 1374-1375 (Fed. Cir. 2021) (expert's analysis unreliable because he "conducted no assessment of the licensed technology versus the accused technology to account for any differences"); *Omega Patents, LLC v. CalAmp Corp.*, 13 F.4th 1361, 1380 (Fed. Cir. 2021) (expert's opinion unsupported because he failed to "account for … distinguishing facts" between licenses and hypothetical negotiation); *see Rude v. Westcott*, 130 U.S. 152, 164 (1889) (settlement payment for alleged infringement "cannot be taken as a standard to measure the value of the improvements patented, in determining … damages").

B. The District Court's Rationale For Allowing The Noncomparable Agreements Does Not Justify Their Admission.

The district court ruled before trial that VLSI could not mention the noncomparable agreements in its opening statement or at any time portray Intel as a "patent holdout" who only pays to license patents when facing litigation, but

deferred ruling on the remaining portions of Intel's *Daubert* and pre-trial motions concerning the noncomparable agreements. Appx4589-4591; Appx4922-4923; Appx2; Appx5. Then, on the last trial day, the court overruled Intel's objections to the noncomparable agreements without any meaningful explanation. Appx2328-2331. After trial, the court denied Intel's post-trial motions on the basis that "the settlement evidence was admitted as proper rebuttal" to Intel's damages case. Appx17-18; *see* Appx95-97; Appx4089-4090; Appx4099-4103. The court's purported justification for allowing this evidence was wrong for several reasons.

For starters, the district court ruled during trial that the noncomparable agreements were admissible ***before*** Intel's damages expert testified. Appx2328-2331. Therefore, contrary to the court's post-trial rationalization, its decision to allow the settlement agreement evidence was not premised on it being "proper rebuttal" to Intel's expert testimony. Appx17-18; *see Dodge v. Cotter Corp.*, 328 F.3d 1212, 1229 (10th Cir. 2003) ("A post-verdict analysis … creates an undue risk of post-hoc rationalization. This is hardly the gatekeeping role … envisioned in *Daubert*[.]"). Moreover, regardless of whether it offered the evidence during its case-in-chief or rebuttal, VLSI—as the party relying on the agreements—was required to establish their comparability. *Omega*, 13 F.4th at 1377, 1381 n.12 ("The patentee has the burden of proving damages, … and where licenses are at issue, that includes 'the burden to prove that the licenses were sufficiently comparable[.]'").

In any event, VLSI's introduction of the noncomparable agreements was in no way "proper rebuttal" to Intel's damages case. Intel's expert Mr. Huston offered a traditional reasonable-royalty opinion that, among other considerations, relied on 20 Intel agreements that he explained were economically and technologically ***comparable*** to the hypothetical license. Appx2364-2366; Appx2769-2784; Appx15394; Appx15406-15408. VLSI's evidence concerning ***noncomparable*** (and unapportioned) agreements simply could not rebut Mr. Huston's analysis based on ***comparable*** agreements. Instead, it improperly "inflate[d] the reasonable royalty analysis with conveniently selected licenses without an economic or other link to the technology in question." *ResQNet.com, Inc. v. Lansa, Inc.*, 594 F.3d 860, 872 (Fed. Cir. 2010).[14]

Nor were the noncomparable agreements appropriate to "lend[] further context to [Intel's] IP licensing practice" or "explain alleged discrepancies between Intel's claimed licensing practices and other Intel licenses that were markedly higher than Intel's expert divulged." *See* Appx18. The only "alleged discrepanc[y]" or purported "licensing practice" was that VLSI thought the amounts Intel had paid to license similar technology on similar terms to the hypothetical license were too low,

[14] In a subsequent trial, the district court acknowledged as much and precluded VLSI from referencing the amounts of these same noncomparable agreements. Appx4357-4373; Appx4433-4437.

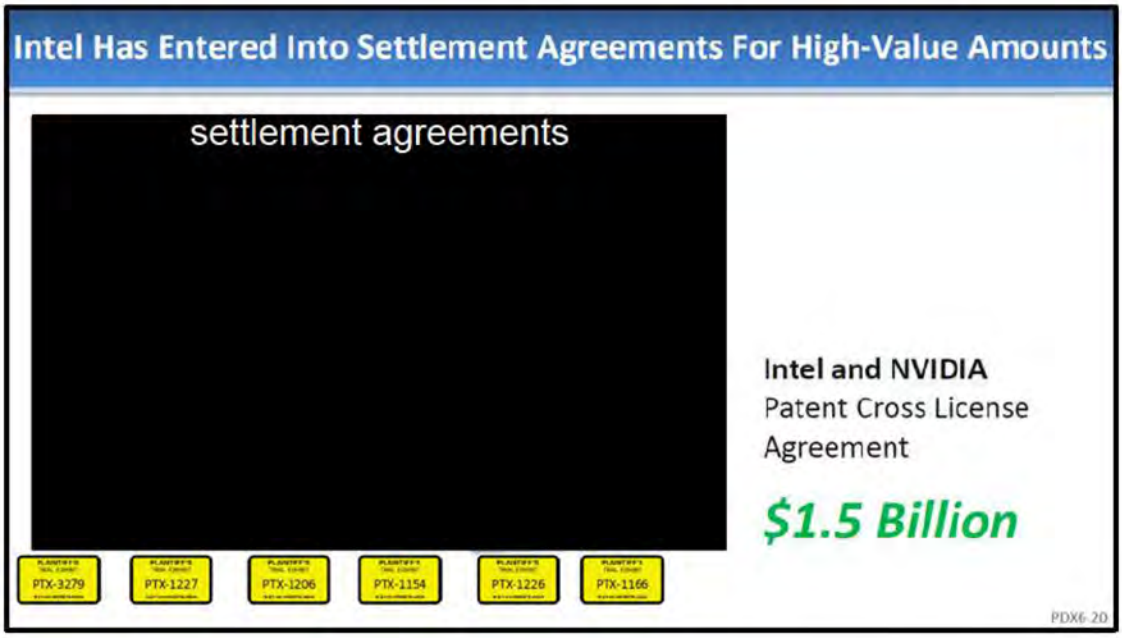
and it wanted to tell the jury about "high-value" amounts Intel had paid to license hundreds of unrelated patents when settling unrelated litigation. *E.g.*, Appx2803-2806. Allowing the noncomparable agreements as "rebuttal" for this purpose turns this Court's precedent upside-down. *Supra* pp. 46-48.[15]

Even if noncomparable agreements could somehow rebut a defendant's supposed licensing practices (they cannot), VLSI's use of the noncomparable agreements still was unduly prejudicial to Intel. Although the district court seemingly accepted VLSI's ruse that Mr. Chandler was not offering "an opinion regarding a specific dollar amount of damages" (Appx18), VLSI and Mr. Chandler repeatedly touted that Intel paid "hundreds of millions of dollars, even billions" under the noncomparable agreements to suggest that Intel should pay similar amounts here. Appx2501; *see* Appx2803-2806; Appx15231-15236; Appx2620-2622.

Notwithstanding the district court's rulings barring VLSI from portraying Intel as a "patent holdout" (Appx2; Appx5), VLSI also used the noncomparable agreements to unfairly suggest that Intel will underpay for a license (or refuse to license) outside of litigation. Appx2502-2503 ("[A] company such as Intel can just

[15] The district court cited only *Intel Corp. v. Tela Innovations, Inc.*, 2021 WL 1222622 (N.D. Cal Feb. 11, 2021), as supporting its reasoning. Appx18. That case—which resulted in summary judgment of no infringement and settled without trial—is non-binding and contrary to this Court's precedent.

simply refuse to reach an agreement and then the patent owner is forced to take them to court to pursue a license."). VLSI then told the jury that, by contrast, Intel pays "high-value amounts" when in litigation:



Appx15231-15236; *see* Appx2516 ("[T]hese were seven agreements when cases have proceeded into litigation, where they've settled for hundreds of millions, if not billions[.]"). As VLSI admitted in pre-trial filings, "Mr. Chandler relie[d] on Intel's settlement agreements as evidence of Intel's patent holdout policies." Appx3615; *see* Appx3775-3776.

VLSI further relied on the Intel settlements to improperly suggest past wrongdoing by Intel. Despite the district court's ruling barring reference to other litigations (Appx5), VLSI emphasized through the noncomparable agreements that Intel paid large amounts to settle prior patent litigations—thereby insinuating that

Intel was a serial infringer. *Retractable Techs. Inc. v. Becton Dickinson & Co.*, 2009 WL 8725107, at *2 (E.D. Tex. Oct. 8, 2009) (excluding reference to prior litigations involving defendant, which could misleadingly suggest defendant had "a character … to violate laws warranting suit").

The verdict underscores just how prejudicial the noncomparable agreements were, as the jury apparently relied on the two largest of those agreements in deciding the damages amounts. Indeed, the jury's $1.5 billion award for the '373 patent matches what Intel paid under the NVIDIA settlement. Similarly, the jury's $675 million award for the '759 patent matches what Intel paid under the Intergraph settlement—an amount not stated at trial but easily discoverable by consulting the *New York Times* as VLSI's counsel suggested to the jury. And as the record demonstrates, at least one juror did consult extra-record sources. *Supra* pp. 20-21.

C. The Erroneous Admission Of The Noncomparable Agreements Requires A New Trial On Liability And Damages.

At minimum, a new damages trial is required because the noncomparable agreements were irrelevant and prejudicial. *LaserDynamics*, 694 F.3d at 77-78 (ordering new damages trial where noncomparable settlement erroneously admitted). A new damages trial is further necessary because the jury's award—which gave VLSI a $2.175 billion windfall for two patents it purchased for an average of about $200,000 each just a few months before filing suit (*supra* pp. 6-

7)—was "clearly excessive." *Giles v. General Elec. Co.*, 245 F.3d 474, 488 (5th Cir. 2001) ("deference [to jury's award] must be abandoned" when "clearly excessive").

Here, however, a new trial is also warranted on infringement and invalidity. That is because the erroneously-admitted noncomparable agreements unfairly painted Intel as a serial infringer and undoubtedly infected the jury's judgment on both liability and damages. *Gasoline Prods. Co. v. Champlin Refining Co.*, 283 U.S. 494, 500 (1931) ("[D]amages … is so interwoven with … liability that the former cannot be submitted to the jury independently of the latter without confusion and uncertainty, which would amount to a denial of a fair trial."); *Williams v. Slade*, 431 F.2d 605, 608-609 (5th Cir. 1970) ("If the decision on the other issues could in any way have been infected by the error then a new trial must be had on all issues.").

V. VLSI'S DAMAGES MODEL SHOULD HAVE BEEN EXCLUDED AND CANNOT SUPPORT THE JURY'S AWARD.

VLSI's expert Ryan Sullivan devised a damages methodology that has never been published, peer-reviewed, presented at a conference, or used in a real-world transaction. Appx1702-1712; *see Daubert v. Merrell Dow Pharms., Inc.*, 509 U.S. 579, 591-595 (1993). His flawed, made-for-litigation methodology allowed VLSI to present a damages claim that vastly overstated any reasonable royalty for the asserted patents. The district court abused its discretion and legally erred by allowing Dr. Sullivan's testimony, which cannot support the jury's award and at minimum requires a new trial. Additionally, this Court should instruct the district

court to determine on remand whether an award of no damages is appropriate given VLSI's waiver of any alternate theory. *Finjan, Inc. v. Blue Coat Sys., Inc.*, 879 F.3d 1299, 1312 (Fed. Cir. 2018) (patentee may receive "no compensation" where it "failed to present a damages case that can support the jury's verdict" and "waived the right to damages based on alternate theories").

A. Dr. Sullivan's Regression Analysis Was Not Tied To The Accused Products And Features.

A reasonable royalty "must reflect the value attributable to the infringing features of the product, and no more." *Omega*, 13 F.4th at 1376. Dr. Sullivan's methodology failed to satisfy this fundamental apportionment principle because his regression model ***included non-accused*** products and features, and ***did not include*** the accused features he sought to value.

Dr. Sullivan used a regression calculation to purportedly measure the impact of 39 selected product features (the independent variables) on product price (the dependent variable) across 6.5 million sales of Intel microprocessor products. Appx1611-1613; Appx15275; Appx3419(¶176); Appx3425(¶186); Appx3488-3491. From this, he concluded that every 1% increase in frequency was associated with a 0.764% increase in price. Appx1613-1614; Appx3438(¶198). Dr. Sullivan then used this number in calculating a reasonable royalty. Appx1654-1657; Appx15290; Appx15292; *supra* pp. 17-18.

Critically, however, Dr. Sullivan's regression analysis was ***not*** based on the value of the Intel product features accused of infringement. Dr. Sullivan admitted that his regression model included ***non-accused products***. Appx3406(¶146) ("I include both accused and non-accused products in the model."); Appx1713-1714. Dr. Sullivan also conceded that his regression model did ***not*** include the features accused of infringing the '373 and '759 patents. Appx1720-1721 (admitting SpeedShift "not included in [his] regression model"); Appx3513(217:14-218:5) (admitting C6SRAM multiplexer not included). Instead, he used 39 ***non-accused features*** as the "independent variables" whose impact he measured in his regression analysis. Appx1612-1613; Appx1713-1723; Appx15275; Appx3488-3491.

Because Dr. Sullivan's regression analysis was based not on the value of the accused features but instead included ***non-accused*** products and features, it cannot support a reasonable royalty. *VirnetX*, 767 F.3d at 1326; *Stragent, LLC v. Intel Corp.*, 2014 WL 12611339, at *1 (E.D. Tex. Mar. 12, 2014) (Dyk, J.) (excluding damages opinion because of "unreliability of [expert's] application of hedonic regression analysis to the facts in this case"); *Coward v. ADT Sec. Sys., Inc.*, 140 F.3d 271, 274-275 (D.C. Cir. 1998) (regression omitting key variables was "so incomplete as to be inadmissible as irrelevant").

The district court denied Intel's *Daubert* motion on this issue without explanation. Appx2; Appx4771-4772; *see* Appx3591-3597. After trial, the court

concluded it had properly admitted Dr. Sullivan's regression analysis, but its generalized reasoning does not withstand scrutiny. Appx19; Appx96-97; *see* Appx4090-4092; Appx4104-4106.

In particular, the district court stated that "hedonic regression … is a 'powerful tool' for 'understand[ing] the relationship between a dependent and an explanatory variable,' and is commonly used." Appx19. While that may be true in some cases, it does not make the specific regression model that Dr. Sullivan applied reliable. *ATA Airlines, Inc. v. Federal Express Corp.*, 665 F.3d 882, 889-896 (7th Cir. 2011) (explaining district court's "responsibility to screen expert testimony" where court admitted testimony based on "regression analysis [being] an accepted model," but there were "grave questions concerning the reliability of [the] application of regression analysis to the facts").

As Intel's regression expert Lorin Hitt explained, regression methods were developed to construct price indices, not to measure the value of individual features in complex products like microprocessors, and several "well-known" difficulties "prevent this approach from reliably estimating the contribution of product attributes to prices." Appx3049(¶53); *see* Appx3051-3054(¶¶62-64). Indeed, there was no evidence that anyone—from Intel, Freescale, NXP, or elsewhere—had ever used a regression analysis to value a patented feature outside litigation. Appx1708-1712; Appx2375; Appx2380-2381. And Dr. Sullivan's specific regression model was

unsuitable for valuing the two features accused of infringement because it included non-accused products and features while failing to include the accused features.[16]

The district court cited (non-binding) cases to support the idea of using regression analysis generally (Appx19), but there is no indication that the regression models in those cases omitted the accused features when calculating patent damages. *See Huawei Techs. Co. v. T-Mobile US, Inc.*, 2017 WL 7052466, at *3 (E.D. Tex. Sept. 10, 2017); *St. Clair Intellectual Prop. Consultants, Inc. v. Acer, Inc.*, 935 F. Supp. 2d 779, 782 (D. Del. 2013); *see also United States v. Valencia*, 600 F.3d 389, 427 (5th Cir. 2010) (wire-fraud case). The court also cited *Bazemore v. Friday*, 478 U.S. 385, 400-401 (1986) (Brennan, J., concurring), but in that employment-discrimination case, the regression analysis accounted for all "major factors" and produced similar results to regression analyses conducted by the defendant, including outside of litigation. Here, by contrast, Dr. Sullivan's regression analysis did not include the features he was trying to value, and no other regression analysis confirmed his opinion.

The district court dismissed Intel's concerns over "Dr. Sullivan's inclusion of non-accused products and features" as going only to "the model's weight, not

[16] Indeed, Dr. Sullivan's misuse of regression analysis led to nonsensical results. *E.g.*, Appx3076-3077(¶¶103-104) (in Dr. Sullivan's model, "supporting faster and more modern" memory "***lowers*** prices by 24%," while "not supporting" encryption feature "***raises*** price by over 79%").

admissibility." Appx19. But Dr. Sullivan's inclusion of non-accused products and features in his regression model, coupled with his failure to include the accused features, rendered his entire methodology unreliable because "a patentee is only entitled to a reasonable royalty attributable to the infringing features." *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 904 F.3d 965, 977 (Fed. Cir. 2018); *see Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1373-1374 (Fed. Cir. 2013) ("District courts, as gatekeepers, must … ensure that all expert testimony is rooted in firm scientific or technical ground[.]").

B. Dr. Sullivan Used Unreliable Inputs From VLSI's Technical Experts.

Dr. Sullivan's damages calculations also directly relied on "inputs" from VLSI's technical experts (Drs. Conte and Annavaram) regarding the alleged benefits attributable to the patents-in-suit. Appx1606-1607; *see* Appx1654-1658; *supra* pp. 17-18. But they, too, were derived from tests that included ***non-accused products and features*** and therefore could not reliably quantify the benefits of only the accused features. These flawed technical inputs provide an independent reason why Dr. Sullivan's damages analysis was unreliable and cannot support the jury's award.

1. Dr. Annavaram's '373-related tests used non-accused products and features.

For the '373 patent, Dr. Annavaram purported to calculate the power savings of the accused C6SRAM multiplexer feature using Intel's Power Model, a

spreadsheet that estimates power characteristics based on thousands of selected inputs. Appx1530-1531; Appx1554; Appx1998. But Dr. Annavaram's methodology had two fundamental flaws.

First, Dr. Annavaram's analysis relied on data from ***non-accused products***. When Dr. Annavaram ran tests to determine which Power Model inputs to select for his calculations, four of the six laptops he tested contained microprocessors not accused of infringing the '373 patent. Appx1555-1557.

Second, Dr. Annavaram's analysis included ***non-accused features***. VLSI's infringement theory related to the "Package C7" sleep state (which uses the accused C6SRAM multiplexer), not the separate "Core C7" sleep state (which does not). Appx1559-1560 ("[Q.] C6 SRAM is not actually used in Core C7, is it? … It's used in the package C7, right? A. It's used in the package. Correct."). But in his laptop tests, Dr. Annavaram mistakenly used data for ***Core C7*** rather than ***Package C7***. Appx1557-1560 ("[Q.] When you bolded Core C7, that was not a correct indication of when C6 SRAM is used, right? A. I guess you could say that[.]"); *see* Appx1975-1976. Indeed, Dr. Annavaram acknowledged that he used Core C7 data "to select … settings in the Intel Power Model," even though Core C7 "does not reflect use of" the accused C6SRAM multiplexer. Appx1578-1581. This error dramatically inflated his power calculations. Appx3548; Appx3132-3133(¶59).

2. Dr. Annavaram's '759-related tests included benefits not attributable to the patented feature.

According to VLSI's damages theory, only a portion of the accused SpeedShift feature's benefits could be allocated to the '759 patent because "[t]he closest non-infringing alternative … would be a processor with Intel's Speed Shift Technology, but without varying the clock frequency of the Ring/Mesh bus." Appx3215(¶1251). Therefore, to "isolate[] the benefits of the [claimed] invention," Dr. Conte asked Dr. Annavaram to "calculate the ***[r]ing bus's*** percentage of power drawn" in Intel's products. *Id.*; Appx1564-1565.

Dr. Annavaram, however, mistakenly ran simulations purporting to calculate the power usage of the ***entire*** "ring domain" rather than just the "ring bus" component. Appx1540-1541. Indeed, Dr. Annavaram acknowledged that he "measured the power consumption of the whole domain," which includes the CBO, last-level cache, and C6SRAM in addition to the ring bus. Appx1564-1566; *see* Appx2726-2727; Appx2740 (Dr. Conte testifying that ring bus is "a member of the ring domain"). By including power savings attributable to more than just the ring bus, Dr. Annavaram necessarily overstated the benefit attributable to the '759 patent—even under VLSI's own damages theory. Appx3560.

* * *

The district court provided no explanation for denying Intel's *Daubert* motions challenging these flawed technical inputs to VLSI's damages model.

Appx1; *see* Appx3537-3548; Appx3554-3563. When it denied Intel's post-trial motions on this issue, the court stated only that "mere conflicting evidence" does not warrant a new trial. Appx19; *see* Appx96; Appx4091-4092; Appx4107-4109. But the errors in Dr. Annavaram's testing make clear that his methodology was not a reliable way to value the alleged benefits of just the patented features. *VirnetX*, 767 F.3d at 1326. This provides an independent basis for why Dr. Sullivan's damages model and calculations—which depended directly on Dr. Annavaram's technical inputs (Appx1606-1607)—should have been excluded and cannot support the verdict. *Uniloc USA, Inc. v. Microsoft Corp.*, 632 F.3d 1292, 1317 (Fed. Cir. 2011) ("[E]xpert[s] … must 'carefully tie proof of damages to the claimed invention's footprint[.]'").

C. VLSI Improperly Sought Disgorgement Of Intel's Profits.

VLSI's damages theory also should have been excluded and cannot support the verdict because it awarded VLSI ***100% of Intel's profits*** allegedly attributable to the asserted patents. Specifically, in his "cost and contribution apportionment" step, Dr. Sullivan reduced the revenues he contended Intel made from the patents-in-suit by subtracting Intel's "total spending" (general and administrative, R&D, and sales/marketing expenses). Appx3461(¶296) ("I calculate the cost apportionment and contribution apportionment by deducting all total spending expenditures from net billings for the accused products."); Appx3473-3474. He then assigned the entire

result—***all*** of Intel's alleged incremental profits—to VLSI as a reasonable royalty. Appx3461-3462(¶¶296-301); Appx3474; Appx1661-1664; Appx3524-3525(303-306); *supra* p. 18.

This 100-0 profit-split in VLSI's favor disgorged Intel's profits, but such disgorgement is not permissible under 35 U.S.C. §284. *Aro Mfg. Co. v. Convertible Top Replacement Co.*, 377 U.S. 476, 505 (1964) (1946 Patent Act amendment "eliminate[d] the recovery of profits … and allow[ed] recovery of damages only"); *Water Techs. Corp. v. Calco, Ltd.*, 850 F.2d 660, 673 (Fed. Cir. 1988) ("[I]nfringer's profits are ***not*** … a measure of the patent[ee]'s damages."). VLSI's damages theory accordingly should have been excluded because it sought a legally-unavailable remedy.

VLSI's proposed profit-split was also factually unsupported. While Dr. Sullivan tried to suggest at trial that his profit-split was closer to 80-20 or 75-25, rather than 100-0 (Appx1661-1664; Appx15301), that is incorrect. Dr. Sullivan reduced Intel's incremental ***revenues*** by 20-25% to account for Intel's total ***spending***, meaning he awarded VLSI 100% of Intel's ***profits*** (revenues minus spending is profits). Appx3461(¶296); Appx3473-3474; Appx1661-1664. But regardless of the exact ratio, Dr. Sullivan identified ***no evidence*** that anyone had ever used his profit-split (whether 100-0, 80-20, or 75-25) to negotiate a license similar to one for the asserted patents. His profit-split analysis was therefore

"arbitrary, unreliable, and irrelevant." *Uniloc*, 632 F.3d at 1318 (vacating damages due to expert's unsupported assumption that parties would agree to 25-75 profit-split); *see VirnetX*, 767 F.3d at 1334 (vacating damages where expert's profit-split "insufficiently tied to the facts").

The district court denied Intel's *Daubert* and post-trial motions, but nowhere addressed Intel's profit-split arguments. Appx2; Appx19; Appx95-97; *see* Appx3597-3600; Appx4091-4092; Appx4106; Appx4962-4963. Because Dr. Sullivan's profit-split theory was legally and factually unsupported, a new trial is required. At minimum, however, this Court should remand for the district court to "articulate its basis for admitting [this] expert testimony[.]" *Rodriguez. v. Riddell Sports, Inc.*, 242 F.3d 567, 581 (5th Cir. 2001); *see Finalrod IP, LLC v. John Crane, Inc.*, 838 F. App'x 562, 563-564 (Fed. Cir. 2021).

D. VLSI's Introduction Of Intel's Total Accused Revenues Violated The Entire Market Value Rule.

VLSI never contended that the patents-in-suit were "the basis for customer demand" for Intel's products; it therefore was not entitled to damages based on the products' entire market value. *LaserDynamics*, 694 F.3d at 67-68. Nevertheless, over Intel's objections (Appx3723-3725; Appx3873; Appx3876-3877; Appx4917-4918; Appx1624-1635), Dr. Sullivan showed the jury that Intel received revenues totaling revenue amount and revenue amount for the '373 and '759 accused products, respectively. Appx1651-1657; Appx15290; Appx15292; Appx13951. He then used

those numbers to defend the revenues he attributed to the patented features as representing only "***a fraction*** – think of it in ***a small piece***, ***a sliver***, if you will, of the overall revenues." Appx1655-1656.

The district court allowed VLSI to introduce Intel's total accused revenues because it deemed them "relevant" to Dr. Sullivan's damages calculations. Appx4918-4920; *see* Appx5; Appx1650-1651. But Dr. Sullivan admitted he did ***not*** need to refer to the total accused revenues to explain his calculations or opinions to the jury. Appx3461-3462(nn.491-493) ("The determination of reasonable royalties herein does ***not*** require disclosure of accused sales[.]"); Appx3749(142-143). And even if "relevant" to some extent, introducing Intel's total accused revenues was unduly prejudicial because it "skew[ed] the damages horizon for the jury" and made VLSI's "proffered damages amount appear modest by comparison." *LaserDynamics*, 694 F.3d at 68; *see Uniloc*, 632 F.3d at 1320 ("[D]isclosure that a company has made $19 billion … from an infringing product cannot help but skew the damages horizon[.]").

After trial, the district court denied Intel's post-trial motions but nowhere addressed how VLSI's introduction of Intel's total accused revenues was proper. Appx19; Appx95-97; *see* Appx4092; Appx4109. Nor could it have, as this was a clear violation of precedent and requires a new trial. *Uniloc*, 632 F.3d at 1320.

VI. THE DISTRICT COURT ERRONEOUSLY DENIED INTEL'S MOTION TO ADD A LICENSE DEFENSE.

Fortress, the company that formed and controls VLSI, acquired control of Finjan Holdings LLC ("FHL") on July 24, 2020. Appx3009. That acquisition triggered Intel's rights under a 2012 Patent License Agreement ("License") to practice patents owned by two FHL subsidiaries ("Finjan Parties") and their "Affiliates." Appx3684(§1.2). Following Fortress's acquisition of FHL, VLSI became an "Affiliate" under the License's plain terms—and Intel became licensed to practice VLSI's asserted patents.

The district court improperly denied Intel leave to amend its answer to add this license defense. Appx65-72. Under FRCP 16(b), courts consider four factors in determining whether to allow amendments after the scheduling order deadline: "(1) the explanation for the failure to timely move for leave to amend; (2) the importance of the amendment; (3) potential prejudice in allowing the amendment; and (4) the availability of a continuance to cure such prejudice." *Meaux*, 607 F.3d at 167-168. The district court legally erred and abused its discretion on all three factors it counted against Intel.

A. Intel's Motion Was Timely.

Intel's explanation for not amending before the scheduling order's March 6, 2020 deadline was clear and compelling: asserting the license defense before the deadline was ***impossible*** because Fortress did not acquire FHL until July 24, 2020.

Intel promptly asserted the license defense after learning of the acquisition. Under the License, Intel was ***required*** to seek resolution of any agreement-related disputes through a mandatory Dispute Resolution Process. Appx3694(§9.3). Intel initiated that process on August 17, 2020, sending notice to Finjan, VLSI, and Fortress. Appx3017-3019.

On September 2, 2020, Intel requested a stay in light of the new license defense. Appx3001-3015. The district court did not rule on that motion, so Intel moved on November 10, 2020—still three months before the trial occurred—to amend its answer "[t]o avoid any doubt that Intel has preserved its [license] defense[.]" Appx3635. The motion also explained that Intel was engaged in the Dispute Resolution Process and, if necessary, intended to move for adjudication of the defense in Delaware, where all parties and issues could be addressed in accordance with the License's forum-selection clause. Appx3635; Appx3637.

Intel thus acted diligently to assert and preserve its rights within the constraints imposed by the acquisition's timing and the License itself. The real delay was the district court's failure to rule on Intel's motion for 16 months.

B. Intel's Amendment Was Not Futile.

Intel's amendment was important because the license provides a complete defense to infringement. Appx68. The district court's conclusion that the defense was nonetheless "futile" directly contradicted a ruling eight months earlier in parallel

Delaware litigation, which held that an identical amendment was ***not futile*** and ***granted*** Intel's motion to add the same license defense. Appx4498; Appx4503-4505 (finding "Intel has been reasonably diligent in seeking to assert its license defense," "VLSI had notice of Intel's position," and "VLSI has not shown that Intel's defense is frivolous or otherwise legally insufficient on its face"). The district court never addressed this conflict and exacerbated the error by disregarding facts alleged in Intel's amended answer and misconstruing Delaware law.

The text and intent of the License are clear: Intel was granted a "perpetual, irrevocable license" to "Finjan's Patents." Appx3687-3688(§3.1). The broad definition of "Finjan's Patents" encompasses all patent rights "owned or controlled" by "Finjan" within the "Capture Period." Appx3685(§1.10).[17] "Finjan" expressly includes Finjan, Inc., Finjan Software, Inc., ***and their "Affiliates."*** Appx3684(Preamble). And "Affiliates" is defined as "any Person that, now ***or hereafter***, directly or ***indirectly*** through one or more entities, controls or is controlled by, or is ***under common control with***, [a] specified Person." Appx3684(§1.2).

Because VLSI and the Finjan Parties are both "Affiliates" under the common control of Fortress, the License's plain language covers VLSI's asserted patents.

[17] The asserted patents undisputedly fall within the Capture Period. Appx3685(§1.4); *see* Appx3684 ("Effective Date").

Indeed, this would have been clear to the sophisticated parties coordinating the transaction:

> Buyer Beware. When a target's contracts purport to bind its affiliates or subsidiaries, the ramifications of an acquisition of … the target may be significant. … Buyer may find that its—and its affiliated entities'—intellectual property is unexpectedly subject to an outgoing license grant on terms it did not negotiate with a party to whom it may not want to be a licensor.

Glazier & Shine, *Acquisitions and IP Licenses: Looking Out for Poison Pill Affiliate*, 249 N.Y.L.J. 2 (2013).

The district court's focus on whether Fortress "own[s] VLSI" was a red herring. Appx70. The License's definition of "Affiliates" depends on "control," not ownership. Appx3684(§1.2). Moreover, the court's statement that "VLSI has no relationship to Finjan whatsoever" (Appx69) was inexplicable given that Intel's amended answer alleged that "VLSI and the Finjan Parties came under the common control of Fortress[.]" Appx3674(¶154). When considering futility, the court was required to accept Intel's allegations, not engage in independent factfinding. *Stripling v. Jordan Prod. Co.*, 234 F.3d 863, 873 (5th Cir. 2000) (applying same "legal sufficiency" standard as FRCP 12(b)(6) "to determine futility").[18]

[18] Discovery in Delaware has confirmed Fortress's common control of VLSI and FHL. *VLSI Tech. LLC v. Intel Corp.*, No. 18-cv-966, Dkt. 846 at 4-8, Dkt. 847 at 2-4 (D. Del.).

The district court also erred when it categorically declared that, under Delaware law, "a non-party to a contract is not bound by that contract." Appx70; *see* Appx3696(§11.4) (License governed by Delaware law). The Delaware Supreme Court held in *In re Shorenstein Hays-Nederlander Theatres LLC Appeals*, 213 A.3d 39, 57 (Del. 2019), that where a signatory was defined to include "an Affiliate of any Member," non-signatory entities satisfying the definition of "Affiliate" were bound by the agreement at issue. The court rejected the argument that "only formal parties … are bound by the terms of the … Agreement" and noted that "[c]ontracts may impose obligations on affiliates." *Id*.[19]

The same rule has been applied in patent cases. In *MicroStrategy Inc. v. Acacia Research Corp*., 2010 WL 5550455, at *12 (Del. Ch. Dec. 30, 2010), the court held that an affiliate formed after a contract's effective date was bound "to the same extent" as the contract's signatory under a definition of "affiliate" similar to

[19] The Chancery Court rulings cited by the district court cannot override the Delaware Supreme Court and, in any event, do not hold that non-signatories are never bound. *See Alliance Data Sys. Corp. v. Blackstone Capital Partners V L.P.*, 963 A.2d 746, 761-762 (Del. Ch. 2009) (contractual provision's plain language did not extend to affiliates); *Sheehan v. AssuredPartners, Inc.*, 2020 WL 2838575, at *9 (Del. Ch. May 29, 2020) (overreading *Alliance Data* and failing to acknowledge *Shorenstein*); *Wenske v. Blue Bell Creameries, Inc*., 2018 WL 5994971, at *5 (Del. Ch. Nov. 13, 2018) (contractual provisions "by their terms, impose[d] no contractual obligation on BB USA"); *Kuroda v. SPJS Holdings, L.L.C.*, 2010 WL 4880659, at *7 (Del. Ch. Nov. 30, 2010) (declining to enforce arbitration agreement "where no parties to the litigation [we]re parties to the Consulting Agreement" and plaintiff made only agency and equitable-estoppel arguments).

the one here. This Court likewise applied a forward-looking definition of "Affiliates" in *Oyster Optics, LLC v. Infinera Corp.*, 843 F. App'x 298, 300-302 (Fed. Cir. 2021), to hold that a patent license extended to a company that became an affiliate after the license was signed.

The district court attempted to distinguish *Oyster Optics* on the ground that the license there benefitted rather than burdened the new affiliate. Appx69. But benefits and burdens are two sides of the same coin. Under Delaware law, "non-signatories may implicitly adopt a contract" and its burdens through "acceptance of the benefits of a contract made for a third-party's benefit." *American Legacy Found. v. Lorillard Tobacco Co*., 831 A.2d 335, 349 (Del. Ch. 2003), *aff'd*, 903 A.2d 728, 745 (Del. 2006). Here, Fortress and its affiliates—including VLSI—have benefitted from the License, including under a provision that prevents Intel from preemptively challenging their patents' validity. Appx3687(§2.5).

In short, the district court came nowhere close to meeting the demanding standard for establishing that Intel's proposed amendment was futile.

C. The Prejudice To Intel In Not Allowing Amendment Is Extreme.

The district court's finding of no prejudice to Intel was based primarily on its flawed futility analysis. Appx71. The court compounded the error by assuming Intel "can pursue a breach of contract claim against Finjan" without any

consideration of Finjan's ability to compensate Intel for the massive damages awarded here. *Id.*

The court further erred by finding that amendment would prejudice VLSI because "[t]rial … has already occurred." Appx71. But Intel filed its motion ***three months before*** the trial occurred, and the district court cannot rely on ***its own 16-month delay*** in addressing Intel's motion to find prejudice. *Cf. In re Quest Diagnostics Inc*., 2021 WL 5230757, at *3 (Fed. Cir. Nov. 10, 2021) (per curiam) (district court erred in relying on intervening activity during delay in ruling on motion as reason to deny transfer); *In re Apple Inc*., 979 F.3d 1332, 1343 (Fed. Cir. 2020) (similar).

* * *

The district court's denial of Intel's amendment was flawed from start to finish. That ruling should be reversed, the judgment vacated, and the district court instructed to allow Intel's license defense.

CONCLUSION

The judgment should be reversed or, alternatively, vacated and remanded for a new trial (if needed) on infringement, invalidity, and damages.

Respectfully submitted,

/s/ William F. Lee

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September 14, 2022

ADDENDUM

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CONFIDENTIAL MATERIAL OMITTED

The material omitted from Appx3-4 contains confidential Intel and third-party licensing information and confidential material regarding VLSI's CEO from a district court order filed under seal; the material omitted from Appx24, Appx43-46, Appx48, Appx55, Appx63-64, Appx77-78, Appx82-83, and Appx85-90 contains confidential Intel technical information from district court orders filed under seal; and the material omitted from Appx96-97 contains confidential Intel financial information from a district court order filed under seal.

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, ***Plaintiff,***	§	
	§	**W:21-CV-00057-ADA**
v.	§	
INTEL CORPORATION, ***Defendant.***	§	

ORDER

In light of the briefs and arguments heard in numerous hearings in the above case the Court enters the following tables that formalize the oral rulings made to date. A short description of the motion along with the corresponding docket numbers and ruling are noted in the tables below.

Dkt.	Description	Decision
252	Intel MSJ re: Indirect & Willful Infringement	**Pre-suit indirect**: Denied **Pre-suit willfulness**: Denied **Post-suit willfulness**: Denied, but VLSI will not be permitted to argue as evidence of willfulness that Intel continued to manufacture products after they were sued. **Enhanced damages**: Denied
253	Intel MSJ re: DOE for '759 Patent	Denied
254	Intel MSJ re: Non-Infringement of '373 Patent	Denied
255	Intel MSJ re: Non-Infringement of '357 Patent	Granted
256	Intel MSJ re: '357 Priority Date	Moot
257	Intel MSJ re: DOE for Six Patents	Denied
261	Intel Daubert for Annavaram re: Power Testing for '373 Patent	Denied
262	Intel Daubert for Conte and Annavaram re: Power Testing for '759 Patent	Denied

263	Intel Daubert for Chandler	Partially Granted (Not allowed to testify on Intel's unwillingness to license absent a lawsuit; with respect to rebuttal, Intel may *voir dire* Chandler to determine his opinion and the basis for his opinion)
264	Intel Daubert for Sullivan	Denied
265	Intel Daubert for Annavaram re: Power Testing of '373 Patent	Denied
266	Intel Daubert re: Innography	Denied
267	Intel Daubert re: Litigation Misconduct	Converted to motions-in-limine, which were Granted
275	VLSI MSJ	**Unclean hands**: Denied **Marking**: Granted (Plaintiff cannot bring in evidence of prior products)
276	VLSI Daubert to Exclude Damages-Related Testimony of Intel Experts	**Pascarella**: Granted **Colwell**: Denied (but VLSI may object if Dr. Colwell says/hints that the patents are not valid or not infringed) **Huston**: Denied (But if Huston tries to address ROI at trial Judge won't let him, and VLSI may object if Mr. Huston says/hints that the patents are not valid or not infringed)
366	Defendant Intel Corporation's Emergency Opposed Motion To Continue Trial	Denied
367	Defendant Intel Corporation's Motion To Stay Court Proceedings	Denied

Dkt.	**MIL**	**Decision**
363	VLSI MIL No. 1.1 – Geographic location of infringement activities.	Granted
363	VLSI MIL No. 1.2 – References to alleged noninfringement alternatives	Granted
363	VLSI MIL No. 1.3 – Indefiniteness arguments not raised during claim construction	Granted, but if the door is opened at trial, the parties are directed to apprise the Court outside of the presence of the jury.
363	VLSI MIL No. 1.4 – Fact witness testimony instructed not to answer	Granted - because irrelevant; fact witnesses may only testify about facts
363	VLSI MIL No. 1.5 – Intel refused to provide testimony	Granted - because irrelevant
363	VLSI MIL No. 1.6 – Hypothetical royalty stacking	Granted, but if the door is opened at trial, the parties are directed to apprise the Court outside of the presence of the jury.
363	VLSI MIL No. 1.7 – Alleged inventor misconduct before the PTO	Granted

364	VLSI MIL No. 2.1 – Fortress expected returns	Granted, but not definitively barred, just need to be given context when it is proffered in order to make a determination at trial.
364	VLSI MIL No. 2.2 – Plaintiff relationship with SoftBank	Intel will not affirmatively offer evidence about SoftBank but may offer such evidence if VLSI opens the door. Intel may discuss VLSI's relationship with Fortress, but disparaging remarks not allowed.
364	VLSI MIL No. 2.3 – Pejorative description of the Plaintiff	Granted (as to both parties).
364	VLSI MIL No. 2.4 – Damages are unprecedented or lottery ticket	Granted
364	VLSI MIL No. 2.5 – How VLSI is paying the cost of the litigation	Granted (as to both parties).
364	VLSI MIL No. 2.6 – Other litigation involving VLSI	Granted (as to both parties).
364	VLSI MIL No. 2.7 – Forum shopping.	Granted
364	VLSI MIL No. 2.7 – Litigation abuse	Granted
364	VLSI MIL No. 2.7 – Western District as a popular venue	Granted
364	VLSI MIL No. 2.8 – Attorney fee agreements between VLSI and its counsel	Granted (as to both parties).
364	VLSI MIL No. 2.9 – Allegations of any discovery abuse including withholding docs or destruction of docs by either party	Granted (as to both parties).
364	VLSI MIL No. 2.10 – [redacted]	Granted
364	VLSI MIL No. 2.10 – State bar claim	Granted
365	VLSI MIL No. 3.1 – Julie Davis	Denied
365	VLSI MIL No. 3.2 – Intel's reputation in the industry	Granted
365	VLSI MIL No. 3.2 – Intel's reputation for innovation	Denied
365	VLSI MIL No. 3.2 – Intel's reputation for philanthropy	Granted (as to both parties).
365	VLSI MIL No. 3.3 – Possibility that damages could be enhanced	Granted
365	VLSI MIL No. 3.4 – Possibility of damages increasing the price of products etc.	Granted
368	VLSI MIL No. 4.1 – Intel's products practicing comparable third party patents	Denied, but going to take it up with relevant witnesses and address it with respect to relevance.

368	VLSI MIL 4.2 - Mr. Huston's [redacted] Hearsay Evidence	Consistent with Intel's statement in its Motion in Limine No. 4 to Exclude Evidence and Argument Regarding [redacted] (D.I. 362 at 7-8 n.4), the parties stipulate that neither Intel nor VLSI will offer any evidence or opinions regarding [redacted] for any purpose in Case No. 6:19-cv-000254, i.e. Case No. 6:21-cv-57.
368	VLSI MIL No. 4.3 – Intel's patents	Intel is allowed to say accurate historical information about their patent portfolio but "Intel is not going to connect, intimate or say explicitly that the fact that they have patents has any impact with respect to the value of your patents" in its opening statement. Intel must raise it with the Court before they put on any expert "who might mention a specific patent." VLSI may then object at that time. A charge to the jury is allowed. Statements that certain patents exist is allowed, but no need to mention they're Intel patents. Intel must notify the court if they plan to discuss one of their patents and VLSI has an opportunity to object. **VLSI notes that Intel has represented they will not be arguing invalidity based on any elected prior art patents.**
368	VLSI MIL No. 4.4 – Patents not valuable because they were not infringed	Resolved by the Court's ruling on VLSI's *Daubert* motion challenging the testimony of Dr. Colwell (D.I. 276).
369	VLSI MIL No. 5.2 – Excluding Intel's experts from relying on hearsay	Denied, but the evidence has to be in the expert reports or trial record for an expert to rely on it as to both sides. If expert relies on a hearsay statement that is not disclosed in the expert's report, evidence of what the declarant said has to be presented at trial.
369	VLSI MIL No. 5.3 – Evidence or argument contrary to claim constructions	Granted as to all sides
369	VLSI MIL No. 5.4 – Predecessor's non-assertion against Intel	Granted
369	VLSI MIL No. 5.5 – Value and propriety of acquiring patents from others	Granted
369	VLSI MIL No. 5.6 – Prior retentions and court rulings in other courts	Granted as to both sides if the door is opened casting experts in a negative light, experts are able to explain why.
370	VLSI MIL No. 6.2 – Absence of Inventors at trial	Intel cannot intimate that VLSI should've/could've brought inventors and they're hiding something unless

		VLSI opens the door (ex. VLSI has testimony that patent made Intel what it is)
369	VLSI MIL No. 5.1 – Lay witness infringement opinions	Granted - fact witnesses may only testify about facts
370	VLSI MIL No. 6.1 – Intel's Alleged Unclean Hands Defense	Granted
370	VLSI MIL No. 6.3 – Disparaging The PTO And Its Examiners	Granted unless door is opened
370	VLSI MIL No. 6.4 – Prosecution history	Denied
370	VLSI MIL No. 6.5 – Withdrawn or narrowed claims	Granted
370	VLSI MIL No. 6.6 – Non-Elected Prior Art	Granted – Relevant to damages, but not a decision on admissibility for other purposes; parties may ask and object to non-elected prior art or individual claim elements - applies to both parties (below) (Intel not going to offer prior art for damages purposes that was not already included in expert reports and parties are instructed to object at trial).
370	VLSI MIL No. 6.7 – Allegations That Individual Claim Elements Were In The Prior Art	Granted (Need to be discussed in the context of damages or obviousness rather than individually) (also see above -applies to both parties).
370	VLSI MIL No. 6.8 – Comparing Accused Products To Prior Art	Objections can be made with respect to admissibility
362	Intel MIL No. 1 – Exclude References to Other Litigations and Proceedings	Granted
362	Intel MIL No. 2 – Exclude References to Discovery Disputes	Granted
362	Intel MIL No. 3 – Exclude References to Intel's Purported Bad Acts and Conduct Outside This Litigation	Granted - unless Intel opens the door
362	Intel MIL No. 5 – Exclude Argument or Testimony That Intel Is a "Patent Holdout"	Resolved by the Court's ruling on Intel's *Daubert* motion challenging the testimony of Mr. Chandler (D.I. 263) and VLSI's representation that it will not refer to Intel as a "patent holdout."
362	Intel MIL No. 6 – Exclude Irrelevant and Prejudicial References to Intel and Processor Industry Financial Performance, Financial Metrics, and Prior Intel Litigation Settlements	Granted - comments about sales about accused products is okay, anything irrelevant to damages calculation is out; sales must be both in expert reports & relevant; settlement agreements cannot be part of either party's opening. After openings, the parties must notify the court prior to discussing any of the settlement agreements so the other party has an opportunity to object.

362	Intel MIL No. 7 – Exclude References to Innography Patent Strength Scores	Denied
362	Intel MIL No. 8 – Exclude Expert Testimony Based on Speculation	Denied, but specifically resolved by the Court's *Daubert* motion ruling (D.I. 267) as to the issue of Professor Conte testifying that "it is quite likely that if he were to examine confidential information from other companies, he'd find the patent widely used, and if he were to examine unaccused Intel products, he'd find that it would -- may be used there as well."
362	Intel MIL No. 9 – Preclude VLSI's Experts From Offering Testimony About Sigmatel, Freescale, or Nxp	Denied, but the parties should limit what they say in opening argument to factual information about these companies.
362	Intel MIL No. 10 – Exclude References to Expert Testimony in Other Cases	Granted
362	Intel MIL No. 12 – Exclude Prejudicial Evidence and Testimony Regarding the Deceased Inventor of the '759 Patent	Denied - may offer that he is dead, but not the details of his death (must be offered in an admissible manner)
362	Intel MIL No. 13 – Exclude Comparisons of Intel Products to Patent Embodiments	Denied.
362	Intel MIL No. 14 – Exclude Comparisons of Burden of Proof Standards	Denied

SO ORDERED.

SIGNED this 19th day of February, 2021.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:21-cv-00057-ADA

JURY VERDICT FORM

3/2/22

12:35

JURY VERDICT FORM

When answering the following questions and filling out this Verdict Form, please follow the directions provided throughout the form. Your answer to each question must be unanimous. Some of the questions contain legal terms that are defined and explained in detail in the Jury Instructions. Please refer to the Jury Instructions if you are unsure about the meaning or usage of any legal term that appears in the questions below.

As used herein, "VLSI" means VLSI Technology, LLC, and "Intel" means "Intel Corporation." As used herein, "'373 Patent" refers to U.S. Patent No. 7,523,373 and "'759 Patent" refers to U.S. Patent No. 7,725,759.

We, the jury, unanimously agree to the answers to the following questions and return them as our verdict in this case:

I. LITERAL INFRINGEMENT

Directions – Question Nos. 1 & 2

In answering the Questions below, please check "**Yes**" or "**No**" for each listed asserted claim in the space provided.

Question No. 1: Has VLSI proven by a preponderance of the evidence that Intel has literally infringed the following asserted claims of the **'373 Patent**? "Yes" is in favor of VLSI, and "No" is in favor of Intel.

'373 Patent

Claim 1:	Yes ✓	No _____
Claim 5:	Yes ✓	No _____
Claim 6:	Yes ✓	No _____
Claim 9:	Yes ✓	No _____
Claim 11:	Yes ✓	No _____

Question No. 2: Has VLSI proven by a preponderance of the evidence that Intel has literally infringed the following asserted claims of the **'759 Patent**? "Yes" is in favor of VLSI, and "No" is in favor of Intel.

'759 Patent

Claim 14:	Yes _____	No ✓
Claim 17:	Yes _____	No ✓
Claim 18:	Yes _____	No ✓
Claim 24:	Yes _____	No ✓

If you have selected "No" for any claim of the '759 Patent listed in Question 2, please proceed to **Question No. 3** for those claims only.

If you have selected "Yes" for all claims of the '759 Patent in Question 2, do not answer Question 3. Please proceed directly to **Question No. 4**.

II. INFRINGEMENT UNDER THE DOCTRINE OF EQUIVALENTS

Directions – Question No. 3

In answering the Question below, please check "**Yes**" or "**No**" for each listed asserted claim in the space provided.

Question No. 3: Answer the following question for each claim of the '759 Patent for which you answered "No" in Question 2 above. Do not answer and leave the form blank for any claim where you answered "yes" in Question No. 2 and found that there was infringement.

Has VLSI proven by a preponderance of the evidence that Intel has infringed the following asserted claims of the **'759 Patent** under the doctrine of equivalents? "Yes" is in favor of VLSI, and "No" is in favor of Intel.

'759 Patent

Claim 14:	Yes ✓	No _____
Claim 17:	Yes ✓	No _____
Claim 18:	Yes ✓	No _____
Claim 24:	Yes ✓	No _____

Please proceed to **Question No. 4**.

III. WILLFUL INFRINGEMENT

Directions – Question No. 4

In answering the Question below, please check "**Yes**" or "**No**" for each listed asserted patent in the space provided.

Question No. 4: Answer the following question for each patent for which you found at least one claim infringed in Questions 1, 2 and/or 3 above. Has VLSI proven by a preponderance of the evidence that Intel's infringement was willful? "Yes" is in favor of VLSI, and "No" is in favor of Intel.

'373 Patent: Yes _____ No ✓

'759 Patent: Yes _____ No ✓

Please proceed to **Question No. 5**.

IV. VALIDITY

Directions – Question No. 5

In answering the Question below, please check "**Yes**" or "**No**" for each listed asserted claim of the '759 Patent in the space provided. This Question is relevant to the '759 Patent only.

Question No. 5: Has Intel proven by clear and convincing evidence that the following asserted claims of the **'759 Patent** are invalid for anticipation by the Yonah Processor alone? "No" is in favor of VLSI, and "Yes" is in favor of Intel.

'759 Patent

Claim 14:	Yes _____	No ✓
Claim 17:	Yes _____	No ✓
Claim 18:	Yes _____	No ✓
Claim 24:	Yes _____	No ✓

Please proceed to **Question Nos. 6-7**.

V. DAMAGES

Directions – Question Nos. 6 & 7

In answering the Questions below, please provide a **dollar amount** in the blank spaces.

Question No. 6: Answer the following question if there is at least one claim of the '373 Patent for which you answered "Yes" in Question 1.

What is the amount of damages you find VLSI has proven by a preponderance of the evidence for Intel's past infringement of the **'373 Patent**?

$ 1,500,000,000.

Question No. 7: Answer the following question if there is at least one claim of the '759 Patent for which you answered "Yes" in either Question 2 or Question 3, and "No" in Question 4.

What is the amount of damages you find VLSI has proven by a preponderance of the evidence for Intel's past infringement of the **'759 Patent**?

$ 675,000,000.

Question No. 8: Is the total amount of damages you found in Questions 6 & 7, 1) a running royalty in the form of a lump sum for past damages only or 2) a lump sum for all damages?

1) Running royalty in the form of a lump sum for past damages only [_____]

-OR-

2) Lump sum for all damages [✓]

You have now reached the end of the verdict form and should review it to ensure it accurately reflects your **unanimous** determinations. After you are satisfied that your unanimous answers are correctly reflected above, your Jury Foreperson should then sign and date this Verdict Form in the spaces below. Once that is done, notify the Court Security Officer that you have reached a verdict. The jury foreperson should retain possession of the verdict form and bring it when the jury is brought back into the courtroom.

I certify that the jury unanimously concurs in every element of the above verdict.

SIGNED this 2 day of March, 2021.

[redacted]

JURY FOREPERSON

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff,*	§	
	§	
	§	**6:21-CV-057-ADA**
v.	§	
	§	
INTEL CORPORATION, *Defendant.*	§	
	§	

ORDER DENYING DEFENDANT INTEL'S RULE 59 MOTION FOR NEW TRIAL

Before this Court is defendant Intel Corporation's Motion for a New Trial pursuant to Fed. R. Civ. P. 59. Intel filed its Motion on April 9, 2021. ECF No. 594. Plaintiff VLSI filed its Reply in Opposition on May 7, 2021. ECF No. 606. After reviewing the parties' briefs and the relevant law, the Court is of the opinion that Intel's Motion should be **DENIED**.

I. FACTUAL BACKGROUND

Plaintiff VLSI filed its suit for patent infringement on April 11, 2019. ECF No. 1 at 1. In its complaint, VLSI accused Intel of infringing U.S. Patent Nos. 8,156,357 ("the '357 Patent"), 7,523,373 ("the '373 Patent"), and 7,725,759 ("the '759 Patent"). The Court held a jury trial, which concluded on March 2, 2021, with a verdict in VLSI's favor. ECF No. 556. The jury awarded over $2 billion in damages to VLSI, and Intel filed its Motion for a New Trial on March 9, 2021. ECF No. 594.

II. STANDARD OF REVIEW

In deciding whether to grant a motion for new trial in a patent case, the law of the regional circuit controls. *Virnetx, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1319 (Fed. Cir. 2014). Accordingly, courts properly grant a motion for a new trial when the movant "clearly establish[es] a manifest error of law" or "present[s] newly discovered evidence." *Simon v. United States*, 891

F.2d 1154 (5th Cir. 1990). Likewise, the jury's determination should not be overturned unless "the verdict is against the great weight of the evidence." *Whitehead v. Food Max of Miss., Inc.*, 163 F.3d 265, 269 (5th Cir. 1998).

Additionally, "mere conflicting evidence or evidence that would support a different conclusion" cannot serve as the basis for a new trial. *Dawson v. Wal-Mart Stores, Inc.*, 978 F.2d 205, 208 (5th Cir. 1992). Indeed, "[u]nless justice requires otherwise, no error in admitting or excluding evidence –or any other error by the court or a party – is grounds for granting a new trial ... at every stage of the proceeding, the court must disregard all errors and defects that do not affect any party's substantial rights." Fed. R. Civ. P. 61.

However, an erroneous jury instruction "may warrant a new trial." *On Demand Mach. Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1337 (Fed. Cir. 2006). In deciding whether to grant a new trial based on an inadequate jury instruction the Court considers whether, using a correct instruction, the jury could have come to only one verdict. *Id.*

III. DISCUSSION

1. No New Trial is Required Because the Court Properly Admitted Probative Evidence and Excluded Irrelevant Evidence.

a. The Court Properly Admitted VLSI's Settlement Agreement Evidence.

Intel urges the Court that it improperly admitted evidence concerning Intel's intellectual property settlement agreement practice, excoriating the testimony as "irrelevant, unfairly prejudicial, and improper rebuttal." ECF No. 594 at 1. Intel further argued that VLSI "[held] back this evidence until after its case-in-chief … allow[ing] VLSI to place large numbers in front of the jury and giv[ing] the false impression of past wrongdoing by Intel." ECF No. 594 at 10. However, the settlement evidence was admitted as proper rebuttal.

At trial, Intel's damages expert offered evidence of licensing agreements Intel believed were comparable to the facts of the situation. ECF No. 606 at 1. In rebuttal, VLSI offered the settlement agreement testimony to explain alleged discrepancies between Intel's claimed licensing practices and other Intel licenses that were markedly higher than Intel's expert divulged. *Id.*

Intel points this Court to *LaserDynamics, Inc. v. Quanta Comput.* to support its argument that the admission of VLSI's rebuttal evidence requires a new trial. ECF No. 594 at 4 – 5; 694 F.3d 51 (Fed. Cir. 2012). However, *LaserDynamics* stands for the proposition that non-comparable settlement agreements cannot support an opinion regarding a specific dollar amount of damages a party is entitled to. 694 F.3d at 77–78. This rule, however, does not extend to the prohibition of non-comparable agreements from lending further context to a party's IP licensing practice. *See Id*; *see also Intel Corp. v. Tela Innovations, Inc.*, 2021 WL 1222622 (N.D. Cal. Feb. 11, 2021) (admitting non-comparable settlement agreements to "shed light on Intel's general licensing practices" because such evidence was not proffered "as the evidence to support the [damages] award").

Additionally, Intel's argument that the settlement agreement evidence "improperly suggest[ed] past wrongdoing by Intel" is unpersuasive. ECF No. 594 at 3. Intel does not cite any portion of the record to support this assertion, and the cases it cites in support are distinguishable. *Sentius Int'l, LLC v. Microsoft Corp.* involved the admissibility of a JMOL decision, not a settlement agreement; likewise *Retractable Techs. v. Becton, Dickinson & Co*. concerned the admissibility of prior litigation. 2015 WL 451950 at *6 (N.D. Cal. 2015); 2009 WL 8725107 at *2 (E.D. Tex. Oct. 8, 2009).

b. The Court Properly Admitted VLSI's Damages Evidence.

Intel also contends that VLSI's damages expert applied methodology "that has never been published, peer reviewed, presented or discussed at a conference, or used in a real-world transaction," dismissing his work as "made-for-litigation." ECF No. 594 at 6–7. However, Intel's arguments merely serve as a restatement of arguments this Court considered and disregarded at the *Daubert* stage.

The hedonic regression analysis used by Dr. Sullivan is a "powerful tool" for "understand[ing] the relationship between a dependent and an explanatory variable," and is commonly used. *United States v. Valencia*, 600 F.3d 389, 427 (5th Cir. 2010); *see also Huawei Techs. Co. v. T-Mobile US, Inc*., 2017 U.S. Dist. Lexis 218166 at *29 (E.D. Tex. Sept. 10, 2017) (acknowledging that regression analysis "adequately approximate[d] the value of the underlying technology"); *St. Clair Intell. Prop. Consultants v. Acer, Inc.*, 935 F. Supp. 2d 779, 782 (D. Del. 2013) (using hedonic regression for damages). While Intel argues that Dr. Sullivan's inclusion of non-accused products and features made his model unreliable and demonstrated a failure to apportion, this argument is properly addressed to the model's weight, not admissibility. *Bazemore v. Friday*, 478 U.S. 385, 400 (1986) (holding that manipulation of regression variables "normally … will affect the analysis' probativeness, not its admissibility").

Intel further argues that VLSI's damages opinion included improper technical inputs to arrive at the final calculation, claiming that premises relied upon by VLSI's experts were contradicted at trial. ECF No. 594 at 10–11. However, "mere conflicting evidence or evidence that would support a different conclusion" cannot serve as the basis for a new trial. *Dawson*, 978 F.2d 205, 208 (5th Cir. 1992).

c. The Court Properly Excluded Intel's Return-On-Investment Evidence.

Moreover, Intel argues that this Court improperly excluded its expert testimony on the reasonable return VLSI could expect from its investment in the asserted patents. ECF No. 594 at 20. Once again, this Court is of the opinion that it properly ruled on the admissibility (or lack thereof) of Intel's ROI expert at the *Daubert* stage – Mr. Pascarella has no experience in determining royalties for processor patents, has never been admitted as an expert in a patent case, and has never performed ROI analysis of the type performed here. *See State Contracting & Eng'g Corp. v. Condotte Am., Inc.*, 346 F.3d 1057, 1073 (Fed. Cir. 2003) (rejecting testimony by expert who "had no experience in placing a value on a patent and did not have any knowledge regarding reasonable royalties). Intel's ROI expert fails to satisfy this threshold question, and therefore was properly excluded.

d. The Court Properly Excluded Evidence Concerning VLSI's Connection to Fortress.

Intel also takes issue with the Court's exclusion of evidence concerning Fortress Investment Group, a non-party hedge fund which controls several smaller funds, some of which own VLSI's parent company. ECF No. 594 at 21. Despite Intel's characterization of the Court's ruling as excluding "all Fortress-related evidence," the Court merely required Intel to obtain clearance from the Court before offering its evidence. When Intel expressed its intent to offer evidence not relevant to any matters of law before the Court, this Court properly excluded the evidence. However, that exclusion fell far short of the blanket prohibition of Fortress-related evidence Intel complains of in its motion.

e. Even if Testimony and Argument Regarding VLSI's CEO Leaving Trial Should Have Been Excluded, No Error Resulted and Intel Waived Its Objection.

Intel lastly objects to the Court's failure to exclude testimony regarding VLSI's CEO leaving trial. ECF No. 594 at 18. Despite Intel's expressed intention to argue the empty chair

regarding CEO Stolarski's leaving trial, when a VLSI witness offered an explanation for Mr. Stolarski's absence, Intel failed to object. Intel failed to object to the testimony when VLSI rested, failed to object when VLSI referenced the testimony and other facts about Mr. Stolarski's absence during closing, and again when Intel renewed its other objections after closing. While Intel successfully objected to the use of a PowerPoint slide referencing Mr. Stolarski's absence, it failed to request a curative instruction. Under these facts, Intel has waived this objection. *United States v. Le*, 512 F.3d 128, 134 (5th Cir. 2007) (finding no error where statements were not objected to, and when an objection was sustained but counsel did not request a curative instruction); *see also Waldorf v. Shuta*, 142 F.3d 601, 629 (3rd Cir. 1998) (acknowledging that "it is clear that a party who fails to object to errors at trial waives the right to complain about them following trial").

2. The Jury Instructions Were Not Erroneous and Therefore Do Not Merit a New Trial.

Intel argues that it was error to instruct the jury that "[u]nlike in a real world negotiation, all parties to the hypothetical negotiation are presumed to believe that the patents are valid and infringed and that both parties were willing to enter into an agreement." ECF No. 594 at 18. However, this instruction was not erroneous. It is well-settled law that the hypothetical negotiation is not a real negotiation. *Mondis Tech. v. LG Elecs.*, 2011 U.S. Dist. LEXIS 78482 at *23 (E.D. Tex. June 14, 2011) (explaining that a "license in the 'real-world' with uncertainty regarding the validity of the patents and infringement" was unlike "the hypothetical negotiation"). Identical instructions have been repeatedly used by this Court and elsewhere. *See MV3 Partners LLC v. Roku, Inc.*, No. 6:18-cv-308-ADA (W.D. Tex.) (same instruction); *SW Holdings, Inc. v. Roku, Inc.*, No. 6:19-cv-44-ADA (W.D. Tex.) (same instruction); *Maxell, LTD. v. ZTE USA Inc.*, 5:16-cv-00179-RWS (E.D. Tex.) (same).

Additionally, Intel argues that the Court's instruction No. 33 is prejudicial due to the inclusion of the word "infringer." However, the damages section of the jury charge, which No. 33 is a part of, admonishes the jury to consider damages *only if* the jury finds against Intel on infringement. Intel's argument that this instruction, which comes from AIPLA's Model Jury Instructions § V.10.3 (2019), is prejudicial, would suggest that all instructions on infringement or damages prejudice the defendant. That plainly is not the case.

IV. CONCLUSION

In sum, Intel has failed to establish a manifest error of law and has not shown the jury's verdict to be beyond the great weight of evidence. The Court properly admitted probative evidence, properly excluded irrelevant evidence, and correctly instructed the jury as to the relevant law. Therefore, Intel's Motion for New Trial is **DENIED**.

SIGNED this 9th day of August, 2021.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff,*	§	
	§	
	§	**6:21-CV-057-ADA**
v.	§	
	§	
INTEL CORPORATION, *Defendant.*	§	
	§	

ORDER DENYING DEFENDANT INTEL'S RULE 52 MOTION FOR JUDGMENT OF NO INFRINGEMENT OF U.S. PATENT NO. 7,725,759 UNDER THE DOCTRINE OF EQUIVALENTS (ECF No. 593)

Before this Court is Defendant Intel Corporation's ("Intel") Motion for Judgment of No Infringement of U.S. Patent No. 7,725,759 under the Doctrine of Equivalents pursuant to Fed. R. Civ. P. 52. Intel filed its Motion on April 9, 2021. ECF No. 593. Plaintiff VLSI Technology LLC ("VLSI") filed its Response in Opposition on May 7, 2021. ECF No. 607. Defendant Intel filed its Reply in Support on May 21, 2021. ECF No. 616. After reviewing the parties' briefs and the relevant law, Intel's Motion is **DENIED** for the reasons set out below.

I. BACKGROUND

Plaintiff VLSI filed its suit for patent infringement on April 11, 2019. ECF No. 1. In its Complaint, VLSI accused Intel of infringing U.S. Patent Nos.7,523,373 ("the '373 Patent") and 7,725,759 ("the '759 Patent"). The Court held a jury trial, which concluded on March 2, 2021, with a verdict in VLSI's favor. ECF No. 556. The jury found infringement of the '759 Patent only under the doctrine of equivalents ("DOE"). ECF No. 593 at 1. The jury awarded over $2 billion in damages to VLSI, which included a $675 million lump sum for infringement of the '759 Patent. Intel filed its Motion for Judgment on April 9, 2021.

The '759 Patent relates to controlling clock frequency in an electronic device. ECF No. 607 at 2. The Patent seeks to "deliver faster clock speeds while also managing power consumption." *Id.* The '759 Patent "discloses and claims a system in which a first master device of a plurality of master devices provides a 'request' to change a clock frequency of a high-speed clock 'in response to a predefined change in performance of the first master device.'" *Id.* at 3. A "programmable clock controller" receives this "request" and provides outputs to independently control (1) a clock frequency of a second master device coupled to a bus, and (2) a variable clock frequency of the bus. *Id.* VLSI asserted that Intel infringed on claims 14, 17, 18, and 24 of the '759 Patent, both literally and under DOE.

VLSI's DOE theory was presented by its expert Dr. Thomas M. Conte. *Id.* at 3. He testified that the combination of core 1 ("first master device") and core 1's associated code in the PCU ("programmable clock controller") provides the claimed "request" in the '759 Patent. *Id.* Specifically, he explained that the core sends a Core_Active signal to the PCU whenever the core becomes active. *Id.* C0 residency counters, which are counters in the PCU, measure the activity of the core over a predefined time interval when [redacted], the code in the PCU generates a "request" for a higher or lower frequency. *Id.* VLSI's literal infringement theory of "request" was based on the Core_Active signals, but its DOE theory was based on the output of the core in combination with the code in the PCU. *Id.* at 4.

Intel now moves for judgment as a matter of law under Rule 52 that Intel does not infringe on the '759 Patent. It argues that three defenses to DOE present questions for the Court to decide: prosecution history estoppel, ensnarement, and claim vitiation. The parties have stipulated that

Intel's defenses are appropriate for resolution pursuant to a bench trial on the papers without any additional live testimony. ECF No. 587.

II. STANDARD OF REVIEW

In a bench trial, "[i]f a party has been fully heard on an issue ... and the court finds against the party on that issue, the court may enter judgment against the party on a claim or defense that, under the controlling law, can be maintained or defeated only with a favorable finding on that issue." Fed. R. Civ. P. 52(c) ("A judgment on partial findings must be supported by findings of fact and conclusions of law as required by Rule 52(a)."). Such findings are made pursuant to Rule 52(a), under which "the court must find the facts specially and state its conclusions of law separately." Fed. R. Civ. P. 52(a). "Rule 52(a) only requires weighing the evidence to determine whether the plaintiff has proven his case." *Thanedar v. Time Warner, Inc.*, 352 F. App'x 891, 897 n.1 (5th Cir. 2009).

In ruling on a Rule 52 motion, the trial court need not consider the evidence in a light favorable to the plaintiff and may render judgment for the defendant if it believes the plaintiff's evidence is insufficient to make out a claim." *Kaneka Corp. v. JBS Hair, Inc.*, 3:10-CV-01430-P, 2013 WL 12190524, at *3 (N.D. Tex. Aug. 30, 2013). Under Rule 52(c), "[a] judgment on partial findings must be supported by findings of fact and conclusions of law as required by Rule 52(a)." Fed. R. Civ. P. 52(c). Rule 52(a) does not require that the district court set out findings on all factual questions that arise in a case. *See Valley v. Rapides Parish Sch. Bd.*, 118 F.3d 1047, 1053-54 (5th Cir. 1997). Rather, the district court is expected to provide a clear understanding of the analytical process by which ultimate findings and conclusions were reached. *Id.* Under Rule 52, the court is "entitled to weigh evidence, make credibility judgments, and draw inferences unfavorable to the [any party]." *Id.* On a Rule 52 motion, the court "make[s] a determination in

accordance with its own view of the evidence." *Fairchild v. All Am. Check Cashing, Inc.*, 815 F.3d 959, 963 n.1 (5th Cir. 2016).

III. FINDINGS OF FACT

The Court makes the following findings of fact.

A. The Parties

1. Plaintiff VLSI is a Delaware limited liability company duly organized and existing under the laws of the State of Delaware. The address of the registered office of VLSI is Corporation Trust Center, 1209 Orange St., Wilmington, DE 19801. ECF No. 1 ¶ 1.

2. Intel is a corporation duly organized and existing under the laws of the State of Delaware, having a regular and established place of business at 1300 S. Mopac Expressway, Austin, Texas 78746. ECF No. 61 ¶ 3.

B. Background of the '759 Patent

3. U.S. Patent No. 7,725,759 was filed June 29, 2005, and is entitled "System And Method of Managing Clock Speed In An Electronic Device." Plaintiff's trial exhibit ("PTX") PTX-5.1. The '759 patent issued on May 25, 2010. *Id.*

4. The '759 patent recognized that one way to increase the performance of an electronic device was to increase the clock frequency of the clock used in the device. "One way to increase the performance of the MP3 player and provide quicker access to stored files is to increase the clock frequency of the clock used in the device." '759 Patent 1:16-19.

5. The inventor of the '759 patent also recognized that increasing performance of the device also increases power consumption. "However, as the clock frequency increases to deliver more performance, the power consumption of the MP3 player also increases." *Id.* at 1:19-21.

6. The inventor recognized that there was a need to balance performance and power to selectively deliver faster clock speeds. "Accordingly, there is a need for an improved system and method of controlling a clock frequency in an electronic device in order to selectively deliver faster clock speeds." *Id.* at 1:22-24.

7. The '759 patent discloses and claims a system in which a first master device of a plurality of master devices provides a "request" to change a clock frequency of a high-speed clock "in response to a predefined change in performance of the first master device." A "programmable clock controller" receives the request and provides outputs to independently control (1) a clock frequency of a second master device coupled to a bus, and (2) a clock frequency of the bus. *Id.* at 8:50-9:4 (claim 14), 9:19-40 (claim 18).

C. Prosecution History of the '759 Patent

8. At trial, VLSI's expert, Dr. Conte, testified that Intel infringes the '759 patent under the DOE by using a combination of a core ("first master device") and the core's associated code in the PCU ("programmable clock controller") to provide the "request" claimed in the '759 patent.

1) The Ansari Reference

9. One of the references cited by the Examiner during prosecution of the '759 patent was U.S. patent No. 7,007,121 to Ansari ("Ansari"). ECF No. 608-4. Ansari is entitled "Method And Apparatus For Synchronized Buses." *Id.* at 1.

10. Figure 6 of Ansari, reproduced below, shows a block diagram of Ansari's system. "FIG. 6 is a functional block diagram illustrating the operation of a bus according to one embodiment of the present invention." *Id.* at 9:59:61; Fig. 6.

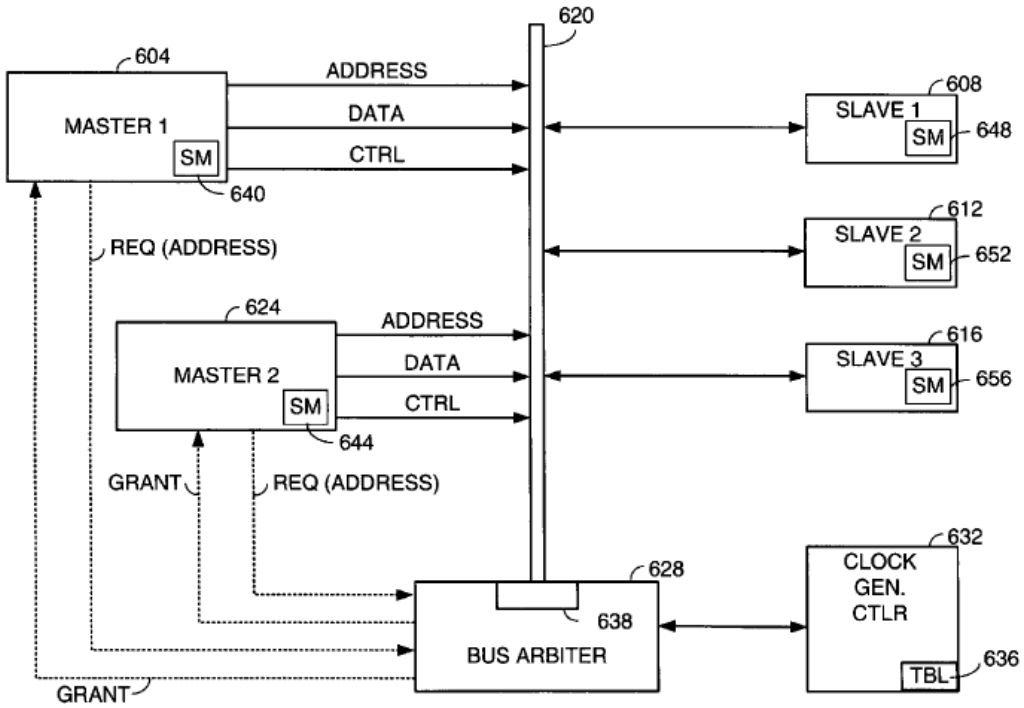

FIG. 6

11. Masters 604 and 624 as well as devices 608, 612, and 616 are coupled to a bus 620. *Id.* at 9:61-65; Fig. 6.

12. Ansari discloses that a master generates a request to a bus arbiter 628 in order to access the bus 620 and initiate a transaction, e.g., to transfer data on the bus to a target device. "In operation, in one embodiment of the present invention, a master, for example, master 624, generates a request to bus arbiter 628 to gain control of bus 620 for a transaction. In addition to generating the request, master 624 specifies an address of a slave to which the communication is to be transmitted." *Id.* at 11:4-9. The masters in Ansari do not request a change (increase or decrease) in the clock frequency of the bus 620.

13. Ansari discloses that the bus arbiter 628 determines the bus speed for the transaction, based on specific parameters. "Because there are at least two masters in the network of FIG. 6, a bus arbiter 628 is required to determine which master 604 or 624 can access and control communications on the bus and a bus rate or speed for the required

transaction. . . . In general, however, the parameters that effect the bus speed include an examination of the source of the communication or transaction, the destination, the length of bus between the two, the number of devices connected to the bus, and other factors such as the relative frequency rates between the two devices." *Id.* at 9:65–10:2, 10:18–23.

14. During prosecution, the Applicant replaced one claim set that recited "at least one" and "the at least one" master device with a new claim set that recited "a" and "the" master device. PTX-8-A.314-.318; PTX-8-A.367-.370.

15. The Applicant did not add any words to the claims such as "only" one master device making a request or the master device "alone" making a request. PTX-8-A.367-.369.

16. The Applicant did not make any arguments during prosecution requiring one master device alone making a request. PTX-8-A.371.

17. The Examiner did not make any statements to convey an understanding that a reference to "a master device" and "the master device" referred to only one master device making a request. PTX-8-A.385. The Examiner simply identified a "Claim Objections" stating: "Claims 30-43 are objected to because of the following informalities: line 6 of claim 30 recite 'the at least one master device' which lacks antecedent basis." *Id*.

18. The following claims were pending as of the Applicant's April 28, 2008 Response: claims 1, 3, 5-15, and 17-29. PTX-8-A.314-.318.

19. Claim 1 recited, in pertinent part: "monitoring a plurality of master devices," "receiving an input from at least one of the plurality of master devices, wherein the input is to *request* an increase to the clock frequency of the bus" and "setting a high frequency flag for the at least one of the plurality of master devices." PTX-8-A.314. Similarly, claim 10 recited, in pertinent part: "receiving a bus master request from at least one of the plurality of devices,

wherein the bus master request is a request to communicate via the bus and to increase the clock frequency of the bus" and "determining whether the at least one of the plurality of devices is a preferred device." PTX-8-A.315. Similarly, independent claim 18 and dependent claim 22 recited, in pertinent part: "at least one master device coupled to the bus" (claim 18) and "wherein the at least one master device provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency" (claim 22). PTX-8-A.316-317.

20. In the Remarks Section of the April 28, 2008, Response, the Applicant distinguished then-pending claim 1 from the Ansari, stating: The cited portions of Ansari fail to disclose or suggest receiving an input from at least one of the plurality of master devices, wherein the input is to request an increase to the clock frequency of the bus, as in claim 1. Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction. *(See e.g.*, Ansari, 8:66, 9:5, 10:30–33). PTX-8-A.319.

21. In other words, the Applicant argued that claim 1 recited "the input is to request an increase to the clock frequency of the bus" and Ansari disclosed a request to *gain access* to the bus rather than request an increase in clock frequency of the bus.

22. The Applicant made a similar argument to distinguish then-pending claim 10 from Ansari, stating:

> The cited portions of Ansari do not disclose or suggest the specific combination of claim 10. For example, the cited portions of Ansari do not disclose receiving a bus master request from at least one of the plurality of devices, wherein the bus master request is a request to communicate via the bus and to increase the clock frequency of the bus and setting a high frequency flag for the at least one of the plurality of devices when the at least one of the plurality of devices is a preferred device, as in claim 10. The Office asserts that Ansari receives a bus master request that is a request to communicate via the bus and references lines 3-17 of column 11. *(See*

> Office Action, page 6). ***Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction.*** (*See* e.g., Ansari, Col. 8, line 66 - Col. 9, lines 5; and Col. 10, lines 30-33). . . . The cited portions of Ansari fail to disclose or suggest that the bus request transmitted by the master 604 or 624 requests an increase to the clock frequency of the bus 620.

PTX-8-A.323 (emphasis added).

23. In response to a further Office Action (PTX-8-A.336-.357), the Applicant cancelled claims 1–29 and introduced new claims 30-58. PTX-8-A.367-.370.

24. New claim 30 recited, in pertinent part: "monitoring a plurality of master devices," "receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device in response to a predefined change in performance of the master device." PTX-8-A.367. New claim 44 recited, in pertinent part: "a master device coupled to the bus, the master device operable to provide a request to change the clock frequency of the bus in response to a predefined change in performance of the master device." PTX-8-A.368. New claim 49 recited, in pertinent part: "a master device coupled to the bus" and "the clock controller operable to receive a request to change the clock frequency of the bus from the master device, the request sent from the master device in response to a predefined change in performance of the master device." PTX-8-A.369.

25. In the Remarks Section of the September 10, 2008, Response, the Applicant distinguished then-pending claim 30 from the cited prior art including Ansari, stating:

> For example, the cited portions of Ansari, Kurosawa, Baek, and Velasco fail to disclose or suggest receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device ***in response to a predefined change in performance of the master device***, as in claim 30. In contrast to claim 30, for example, Ansari discloses receiving a request from a device that happens to cause an arbiter to increase the bus speed. However, a request from a device that happens to cause an arbiter to increase the bus speed is not a request to change the bus speed.

PTX-8-A.371 (emphasis added).

26. Applicant's Response makes clear that Applicant was distinguishing Ansari because the master in Ansari did not send a request "in response to a predefined change in performance of the master device."

27. Furthermore, the Applicant argued, consistent with its September 17, 2007, and April 28, 2008 Responses, that the master device in Ansari does not request a change of the bus clock speed. In other words, the master in Ansari simply requests access to the bus to initiate a bus transaction, and that it is the bus arbiter that may increase the clock speed of the bus. At no point did the Applicant distinguish Ansari for purportedly disclosing a first master device and a programmable clock controller (or any other device) that, in combination, provided the claimed request. Nor did the Applicant argue that the then-pending claims required only the first master device alone to make the claimed request.

28. When Applicant introduced new claim 30 in the September 10, 2008, Response, it erroneously used the old formulation "from the at least one master device" in the last limitation of claim 30, despite reciting "a master device" earlier in the claim.

30. (New) A method of controlling a clock frequency of a bus, the method comprising:

monitoring a plurality of master devices coupled to the bus;

receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device in response to a predefined change in performance of the master device; and

in response to receiving the request from the at least one master device, controlling the clock frequency of the bus.

PTX-8-A.367 (highlighting added for emphasis).

29. In a subsequent Office Action, the Patent Office noted this minor error, stating "Claims 30-43 are objected to because of the following informalities: line 6 of claim 30 recite

'the at least one master device', which lacks antecedent basis." PTX-8-A.385. There were no statements by the Examiner that the claims necessarily refer to *only* one master device making the request. *Id*.

30. In a subsequent Response, the Applicant corrected the minor error by amending claim 30 to recite "in response to receiving the request from the at least one master device." PTX-8-A.405. In the Remarks section, the Applicant stated: "The Office has objected to claims 30-43 because of informalities. Applicant has amended the claims to cure the informalities." PTX-8-A.410. There were no statements by the Applicant that the amended claims necessarily refer to *only* one master device making a request. *Id*.

31. The following claims were pending as of the Applicant's September 17, 2007, Response: claims 1, 3, and 5–29. PTX-8-A.235-.239.

32. Then-pending independent claim 1 in the September 17, 2007 Response recited:

1. (Currently Amended) A method of controlling a clock frequency, the method comprising:

monitoring a plurality of master devices coupled to a bus within a system;

receiving an input from at least one of the plurality of master devices, wherein the input is to request an increase to the clock frequency of the bus;

determining whether to enable the request to increase the clock frequency of the bus and,

setting a high frequency flag when the request is enabled;

monitoring a plurality of high frequency flags; and

selectively increasing a clock frequency in response to at least one of the plurality of high frequency flags being set.

PTX-8-A.235 (highlighting added for emphasis). Then pending independent claim 10 recited a similar limitation. PTX-8-A.236.

33. In its September 17, 2007, Response, the Applicant explained that Ansari sends a bus request to initiate a transaction on the bus, not to request an increase in frequency, and that

it is the bus arbiter that determines an appropriate frequency to use for the transaction. "A master device seeking bus resources to initiate a transaction sends a bus request and a destination address to the bus arbiter so that the arbiter can determine a corresponding bus frequency. (Col. 8, line 66 to col. 9, line 6). Thus, in Ansari, a master device sends a bus request to the bus arbiter. The master device does not determine or request a desired bus frequency because it is the bus arbiter that determines the bus frequency based on various factors." PTX-8-A.241-.242 (emphasis added).

34. Thus, consistent with Ansari's teaching, the Applicant argued that the masters in Ansari only request access to the bus to initiate a transaction, such as a data transfer.

35. In the Remarks Section of the April 28, 2008 Response, the Applicant distinguished then-pending claim 1 from the Ansari, stating:

> The cited portions of Ansari fail to disclose or suggest receiving an input from at least one of the plurality of master devices, wherein the input is to request an increase to the clock frequency of the bus, as in claim 1. Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction. (*See* e.g., Ansari, Col. 8, line 66 - Col. 9, lines 5; and Col. 10, lines 30-33).

PTX-8-A.319.

36. In other words, Applicant argued that claim 1 recited "the input is to request an increase to the clock frequency of the bus" and Ansari disclosed a request to *gain access* to the bus rather than request an increase in clock frequency of the bus.

37. The Applicant made a similar argument to distinguish then-pending claim 10 from Ansari, stating:

> The cited portions of Ansari do not disclose or suggest the specific combination of claim 10. For example, the cited portions of Ansari do not disclose receiving a bus master request from at least one of the plurality of devices, wherein the bus master request is a request to communicate via the bus and to increase the clock frequency of the bus and setting a high frequency flag for the at least one of the plurality of

> devices when the at least one of the plurality of devices is a preferred device, as in claim 10. The Office asserts that Ansari receives a bus master request that is a request to communicate via the bus and references lines 3-17 of column 11. *(See* Office Action, page 6). ***Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction.*** (*See* e.g., Ansari, Col. 8, line 66 - Col. 9, lines 5; and Col. 10, lines 30-33). . . . The cited portions of Ansari fail to disclose or suggest that the bus request transmitted by the master 604 or 624 requests an *increase* to the clock frequency of the bus 620.

PTX-8-A.323.

38. Applicant's arguments in the April 28, 2008, Response were consistent with what Applicant argued in its September 17, 2007, Response.

39. In the Remarks Section of the September 10, 2008, Response, the Applicant distinguished then-pending claim 30 from the cited prior art including Ansari, stating:

> For example, the cited portions of Ansari, Kurosawa, Baek, and Velasco fail to disclose or suggest receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device in response to a predefined change in performance of the master device, as in claim 30. In contrast to claim 30, for example, Ansari discloses receiving a request from a device that happens to cause an arbiter to increase the bus speed. However, a request from a device that happens to cause an arbiter to increase the bus speed is not a request to change the bus speed.

PTX-8-A.371 (emphasis in original).

40. The Applicant was distinguishing Ansari because the master in Ansari did not send a request "in response to a predefined change in performance of the master device." Furthermore, the Applicant argued, consistent with its September 17, 2007, and April 28, 2008, Responses, that the master device in Ansari does not request a change of the bus clock speed. In other words, the master in Ansari simply requests access to the bus to initiate a bus transaction, and that it is the bus arbiter that may increase the clock speed of the bus.

D. VLSI's Infringement Claims in This Litigation

41. VLSI's infringement claims have not shifted during the litigation.

42. In its complaint for patent infringement, VLSI accused "Intel products that use infringing Hardware-Controlled Performance States ('HWP' or 'Speed Shift') technology" infringe at least claim 1 of the '759 patent both literally and under the doctrine of equivalents. ECF No. 1.

43. In its July 22, 2019, Preliminary Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, and Cannon Lake. ECF No. 592-4.

44. In its January 2, 2020, Amended Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, and Whiskey Lake. ECF No. 592-5.

45. In its January 2, 2020 Amended Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, and Whiskey Lake. *Id.*

46. In its January 26, 2020 Second Amended Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel

products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, Whiskey Lake, Comet Lake, Ice Lake, and Tiger Lake. ECF No. 592-6. VLSI asserted both literal infringement and infringement under the doctrine of equivalents. *See, e.g., id*., at 27, 84, and 131.

47. In its January 31, 2020 Final Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, Whiskey Lake, Cascade Lake, Comet Lake, Ice Lake, and Tiger Lake. ECF No. 592-7. VLSI asserted both literal infringement and infringement under the doctrine of equivalents. *See, e.g., id*., at 27–28, 93, and 148.

48. In the December 22, 2020 Joint Final Pretrial Order, VLSI asserted that "Intel infringes Claims 1, 14, 17, 18, 24, and 26 of U.S. Patent No. 7,725,759 by making, using, selling, offering for sale, and/or importing into the United States Intel's Skylake client and server processors, Kaby Lake processors, Coffee Lake processors, Whiskey Lake processors, Amber Lake processors, Comet Lake processors, Cannon Lake processors, Cascade Lake server processors, Ice Lake client and server processors, and Tiger Lake processors, all other Intel products that include Intel's Speed Shift Technology, and any other processors with essentially the same structures as those identified in VLSI's infringement analysis ("'759 Accused Products"). Intel infringes Claims 1, 14, 17, 18, 24, and 26 of the '759 Patent, directly

or indirectly, either literally or under the doctrine of equivalents. The doctrine of equivalents is available and has been properly applied for the Asserted Claims." ECF No. 398-02 at 7.

49. During discovery, Intel only asserted prosecution history estoppel and ensnarement defenses. Intel first raised the issues of alleged ensnarement for the '759 Patent on April 17, 2020, generally asserting that: "Further, VLSI's doctrine-of-equivalents theories cannot be asserted because they would ensnare the prior art" followed by a general listing of the same prior art asserted by Intel in its invalidity contentions. *See* ECF No. 608-7.

50. Additionally, despite raising the issue of claim vitiation for other patents in April 2020, Intel did not amend its responses ever to include such an assertion for the '759 patent. *See* ECF No. 608-7 at 269–287.

51. Further, Intel only sought responses to its assertion of ensnarement on June 17, 2020, the last possible day to serve written discovery, when it served its Third Set of Interrogatories. In Interrogatory No. 22 it asked: "If You contend that the doctrine of ensnarement does not bar VLSI from obtaining relief for Intel's alleged infringement of any of the Asserted Patents, set forth the complete basis for each and every such contention on a patent-by-patent basis." ECF No. 608-9 at 3. VLSI responded by explaining how Intel's vague assertion of ensnarement was insufficient and that its infringement theories, as memorialized in its highly detailed infringement contentions, demonstrate that no prior art is "ensnared." ECF No. 608-10 at 64–65.

52. Intel never sought responses to any claims of prosecution history estoppel or claim vitiation.

53. VLSI preemptively responded to Intel's allegations in expert discovery. In his Opening Report, Dr. Conte addressed ensnarement and provided an implicit hypothetical claim through his doctrine of equivalents analysis. ECF No. 608-2 ¶¶ 616, 638, 1057, 1077.

54. Intel set forth its general ensnarement, prosecution history estoppel, and claim vitiation defenses in the Rebuttal Report of Dr. Dirk Grunwald, which did not allow for VLSI to address these assertions made by Dr. Grunwald for the first time in a written report. Dr. Grunwald's Opening Report did not include an assertion of any of these defenses.

55. VLSI provided Intel with notice of a hypothetical claim that would both literally capture the accused products but not the vaguely asserted prior art. *See, e.g., id.* ¶¶ 613-639, and 1054–1078.

56. Intel filed a motion for summary judgment of no infringement under the doctrine equivalents on the basis of prosecution history estoppel only. *See* ECF No. 253. Intel did not assert claim vitiation or ensnarement as defenses in its motion.

57. In the Joint Pre-Trial Order, Intel reasserted its assertions of prosecution history estoppel, ensnarement, and the "all elements" rule. ECF No. 398-02 ¶ 41; *see also id.* ¶ 77. Intel did not list any prior art specific to ensnarement, but listed Yonah, Chen, Terrell, Rusu, and Kiriake as prior art for anticipation and/or obviousness. *Id.* ¶ 42. VLSI responded that it disagrees with Intel's contentions. *Id.* ¶ 19.

58. During fact discovery, VLSI asserted that Intel products infringe claims of the '759 patent under the doctrine of equivalents. For example, in its January 31, 2020, Final Infringement Contentions, VLSI identified that Intel products (including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, Whiskey Lake, Cascade Lake, Comet Lake, Ice Lake, and Tiger Lake) infringe claims of the '759 patent under the doctrine of equivalents.

ECF No. 592-7 at 2728, 48, 53–54, 59–60, 66–67, 93, 116, 147–148, 165–166, 175–176, and 185.

59. For example, VLSI asserted: "In the Accused Products, for instance, requests within the PCU to change the frequency of the clock achieve substantially or exactly the same function (e.g., to change the clock frequency of the clock in response to a predefined change in performance of a master device as configured in the Accused Products) in substantially or exactly the same way as set forth in the claim (e.g., by using circuitry/logic in the master device and/or PCU of the Accused Products), to achieve substantially or exactly the same result (e.g., control the clock frequency of a second master device coupled to the bus as implemented in the Accused Products)." ECF No. 592-7 at 93, 147–148.

60. VLSI's technical expert, Dr. Conte, asserted that Intel products infringe claims of the '759 patent under the doctrine of equivalents. ECF No. 608-2 ¶¶ 613-639 and 1054–1078.

61. For example, Dr. Conte explained that the "Accused Products perform the substantially the same/identical function as recited in the claim in substantially the same way, namely, by using the combination of a core and the PCU to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device . . . ." *Id.* ¶ 616.

62. In his expert report on infringement of the '759 patent, Dr. Conte, explained that under the doctrine of equivalents the combination of the core and the PCU provides the claimed request. "The Accused Products perform the substantially the same/identical function as recited in the claim in substantially the same way, namely, by using the combination of a core and the PCU to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device . . . ." *Id.* ¶ 616.

63. Dr. Conte's analysis in his expert report identified a hypothetical claim in support of his doctrine of equivalents theory, namely, "by using the combination of a core and the PCU to provide a request." *Id.*

64. Dr. Conte expressly addressed ensnarement in his expert report, stating that the manner in which he was reading the claim did not ensnare the prior art.

> 638. My application of this claim term under the doctrine of equivalents does not encompass the prior art. I have read Intel's interrogatory response where it assert that "VLSI's doctrine-of-equivalents theories cannot be asserted because they would ensnare the prior art." 06- 24-2020 Intel Response to Interrogatory No. 15, at 519; see also id., at 520-536. I disagree. As an initial matter, Intel has not provided any explanation or analysis for how the doctrine of ensnarement could allegedly bar my analysis of infringement under the doctrine of equivalents (and, in fact, the doctrine does not bar it). For example, the manner in which I am reading this claim term on the '759 Accused Products differs from the teaching of the alleged prior art cited by Intel. By way of another example, my opinions herein under the doctrine of equivalents do not ensnare the cited prior art at least because Intel's cited prior art fails to teach, alone or in combination, other claim terms as well as the claimed combinations recited the claims of the '759 patent. I expect that I will address the reasons why the cited prior art fails to anticipate or render obvious the claims of the '759 patent in response to any report from an Intel expert on the topic.

Id. ¶ 638.

E. Hypothetical Claim

65. The following is a hypothetical claim presented by VLSI that is based on claim 14 of the '759 patent, with additions thereto shown in underline text and deletion shown in strikethrough text.

> Hypothetical Claim. A system comprising: a bus capable of operation at a variable clock frequency; a first master device coupled to the bus, the first master device or the first master device and its associated code in a programmable clock controller configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and the ~~a~~ programmable clock controller having an embedded computer program therein, the computer program including instructions to: receive the request provided by the first master device or the first master device and its associated code in the programmable clock controller; provide the clock

> frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller; and provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller.

66. VLSI's technical expert, Dr. Conte, testified at trial that Intel's accused products infringe under the doctrine of equivalents consistent with the scope of the foregoing Hypothetical Claim. Sealed Trial Tr. 36:3-61:23, Trial Tr. 487:17-488:10, 1417:25-1420:1; ECF No. 553-02 PDX4.154-214, PDX4.216-220; ECF No. 553-03 PDX5.13.

67. Intel's expert, Dr. Grunwald, never asserted Terrell, Ansari, or any obviousness combination at trial.

F. This Court Previously Rejected Intel's Arguments on Prosecution History Estoppel

68. Intel previously raised the same arguments with respect to prosecution history estoppel in its Motion for Summary Judgment of No Infringement Under the Doctrine of Equivalents. *See* ECF No. 253. Specifically, Intel argued that the Applicant narrowed the claims during prosecution and as such VLSI was barred from asserting the doctrine of equivalents.

69. This Court rejected Intel's arguments—the same arguments raised in Intel's Rule 52 Motion—finding that Intel had not proven its defense of prosecution history estoppel. ECF Nos. 411, 507.

G. VLSI's DOE Case at Trial

70. At trial, VLSI's expert, Dr. Conte, testified that Intel infringed claims 14, 17, 18, and 24 of the '759 patent, both literally and under the doctrine of equivalents. Sealed Trial Tr. 36:3-61:23, Trial Tr. 487:17-488:10, 1417:25-1420:1; ECF No. 553-02 PDX4.154-214, PDX4.216-220; ECF No. 553-03 PDX5.13.

71. At trial, Dr. Conte testified that the claimed "master device" was the cores in the Intel accused products. Sealed Trial Tr., 38:20-22; ECF No. 553-02 PDX4.166-167, PDX4.174.

72. Dr. Conte further testified that the claimed "request" was the Core_Active signal provided by the core(s) in the Intel accused products. Trial Tr. 417:17-23, 474:5-8; Sealed Trial Tr., 39:23-40:7, 40:18-41:8, 42:13-43:9; ECF No. 553-02 PDX4.171-174.

73. Dr. Conte testified that the Core_Active signal is sent by a core in response to a predefined change in performance of the core, [redacted]. "Q. Okay. So is there a request as required by the claims? A. There is. So the way it works is that workload changes . . . . You launch Word, and it runs on a core. [redacted] Sealed Trial Tr. 39:23-40:7; PTX-1805; *see also* Sealed Trial Tr. 42:13-43:4; ECF No. 553-02 PDX4.171-172:

[redacted]

74. Dr. Conte further testified that the claimed "programmable clock controller" included, among other circuitry, the PCU in Intel's accused products. Sealed Trial Tr., 40:18-23; ECF No. 553-02 PDX4.178-184.

75. Dr. Conte testified that Intel's accused products also infringe claims 14, 17, 18, and 24 of the '759 patent under the doctrine of equivalents. Sealed Trial Tr., 52:21-24, 57:21-58:1, 61:18-23; ECF No. 553-02 PDX4.202-214, PDX4.224.

76. Dr. Conte testified that the "core and the Core 1's P-code . . . provides the same function as required by the master device in the claim, that is to provide a request." Sealed Trial Tr., 55:1-6; 53:14-56:3; ECF No. 553-02 PDX4.204-214.

77. Dr. Conte further testified that "[t]he claim says 'the first master device provides a request.' Now, it's the first master device and its P-code that provides the request." Sealed Trial Tr., 55:7-11.

78. Dr. Conte testified that Intel's documentation also calls what Dr. Conte points to as the request, namely the output of a core's P-Code, as "a request for higher or lower frequency."

[redacted]

Sealed Trial Tr., 54:9-22; ECF No. 553-02 PDX4.205-208, PDX4.210.

79. [redacted]

[redacted],

[redacted] PTX-3484.3.

80. Dr. Conte further testified that the PCU's decision instructions treats the output of the core's P-Code as requests.

Sealed Trial Tr., 56:7-57:7; D-1154.

81. Dr. Conte testified that he applied the function-way-result test for his doctrine of equivalents opinions. "Q. Okay. So now, let's go back to your Doctrine of Equivalents analysis. Did you apply the function/weigh/result test? A. I did. . . ." Sealed Trial Tr., 55:1-6; ECF No. 553-02 PDX4.202.

82. Dr. Conte testified that Intel accused products "provides the same function as required by the claim ,that is to provide a request." Sealed Trial Tr., 55:4-6; Dkt. ECF No. 553-02 PDX4.208.

83. Dr. Conte testified that Intel's accused products provide a literal request in substantially the same way as the claim. Sealed Trial Tr., 55:1-11. Dr. Conte testified that the different between Intel's products and the claim is "just a difference of where an engineer draws this [dotted] line" and that it is "a design choice." Sealed Trial Tr., 55:12-17; ECF No. 553-02 PDX4.207, -.209:

[redacted]

84. Dr. Conte testified that "the result is that a request is provided" and that the Intel accused products provide "the same result as required by the claim." Sealed Trial Tr., 55:18-20, 56:3; ECF No. 553-02 PDX4.210.

85. Dr. Conte testified that the [redacted] within the PCU receives the request from the core and its P-code. Sealed Trial Tr., 56:4-57:16; ECF No. 553-02 PDX4.207; D-1154.

86. Dr. Conte did not identify C0 residency counters as a "request" under his DOE analysis at trial. Dr. Conte, instead, explained how C0 residency counters in Intel's products

[redacted]

87. Dr. Conte further testified that "[i]nside the PCU are these counters. They're called C0 residency counters. And the way they work is that Core_Active sends a signal to the PCU, and that starts these counters counting." Trial Tr. 1419:2-8; ECF No. 553-02 PDX5.13.

88. Dr. Conte explained the relationship between C0 Residency and the Core_Active signal, stating: "The core sends Core_Active signal and that starts this counter counting. And that's measured in this activity window we talked about." Trial Tr. 1419:12-18; ECF No. 553-02 PDX5.13.

89. Dr. Conte testified that "those [C0 residency] counters are going to be adjusted because you get the . . . Core_Active signal from the cores." Trial Tr. 1453:15-22.

90. Dr. Conte testified that "Core_Active starts these C0 residency counters. And then you send an inactive, it stops them." Trial Tr. 487:24-488:3.

91. Dr. Conte testified that the "Core_Active" signals are not sent periodically, but are sent "whenever the core becomes active." Trial Tr. 488:4-7 ("Q. Are Core_Active signals sent periodically? A. No. Q. When are they sent? A. They're sent whenever the core becomes active.").

92. Dr. Conte testified that the "testimony about periodic signals" do not "apply to the Core_Active requests." Trial Tr. 488:8-10 ("Q. So does any of that testimony about periodic signals apply to the Core_Active requests? A. No.").

93. Dr. Conte further testified how the C0 residency counters change, stating: "These counters change as you go through these windows. So imagine you start at the window with a five in one of those counters; and you go all the way to the end of the window, and at the end, it's five. Then you go to the next window, and during the next window there's a Core_Active and it goes six, seven, eight, nine, ten, and then you end. So what Dr. Rotem is not considering a request is really the fact that the counter from this window to this window actually changes. But if you recall, there was a lot of talk about that on Tuesday. And I said that that's indicative of a request." Trial Tr. 1454:14-1455:4.

94. Dr. Conte disputed Dr. Grunwald's demonstrative DDX-10.26 regarding the operation of Speed Shift, and modified Dr. Grunwald's demonstrative to show the relationship between Core_Active signal sent by the core and the C0 Residency counter in the PCU. Trial Tr. 1419:2-14:20:1; ECF No. 553-02 PDX5.13:

95. Dr. Conte testified that the "Core_Active then [is] an input to the autonomous algorithms that calculate the speed of the cores" and that "[i]f you didn't have that signal to turn on the counters, the PCU would never know that the cores' load changed. It would never change the speed of the cores due to loading." Trial Tr. 1419:19-1420:1.

96. At trial, Intel engineer, Dr. Efraim Rotem, testified that there are people at Intel that write the P-code for the PCU and identified Mr. Dan Borkowski. Dr. Rotem did not identify himself as writing P-code for the Intel accused products. Trial Tr. 1088:4-14.

97. At trial, Dr. Rotem never addressed or responded to Dr. Conte's testimony regarding the Core_Active signal sent by the cores to the PCU as part of the Dr. Conte's literal and doctrine of equivalents infringement analyses. *See generally* Trial Tr. 1045-1135 (Rotem Trial Testimony).

98. At trial, Intel engineer, Dan Borkowski, testified that "[w]e write the code, the P-code." Sealed Trial Tr. 96:20-21; Trial Tr. 1138:5-13.

99. At trial, Mr. Borkowski never addressed or responded to Dr. Conte's testimony regarding the Core_Active signal sent by the cores to the PCU as part of the Dr. Conte's literal and doctrine of equivalents infringement analyses. *See generally* Sealed Trial Tr. 96:8-108:7; Trial Tr. 1136-1153 (Borkowski Trial Testimony).

H. At Trial, the Jury Found Infringement of the '759 Patent Under the Doctrine of Equivalents

100. The jury found that Intel has infringed claims 14, 17, 18, and 24 of the '759 patent under the doctrine of equivalents. ECF No. 564 at 3.

IV. ANALYSIS

Having made its findings of fact, the Court now turns to the merits of Intel's Motion. Intel argues that VLSI is barred from relying on a DOE theory. Even if there is no literal infringement, DOE may constitute infringement if the differences between a claim limitation and the accused product are insubstantial. *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 24 (1997). Intel argues that VLSI's DOE claim is legally barred for three independent reasons: prosecution history estoppel, the ensnarement doctrine, and claim vitiation. These three arguments are addressed below.

A. Prosecution history estoppel does not bar VLSI's doctrine of equivalents theory.

A patent's prosecution history can legally bar application of a DOE claim in two ways: "(1) by making a narrowing amendment to the claim ('amendment-based estoppel) or (2) by surrendering claim scope through argument to the patent examiner ('argument-based estoppel')." *Amgen Inc. v. Coherus BioSciences Inc.*, 931 F.3d 1154, 1159 (Fed. Cir. 2019).

1) VLSI's amendment to the '759 Patent does not trigger the application of amendment-based prosecution history estoppel.

Amendment-based estoppel "arises when an amendment is made to secure the patent and the amendment narrows the patent's scope." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 736 (2002). "[The doctrine] applies when a claim is amended for 'a substantial reason related to patentability,' including 'to avoid the prior art . . . .'" *GeoTag, Inc. v. Starbucks Corp.*, No. 2:10-CV-572-MHS-RSP, 2014 WL 12639927, at *2 (E.D. Tex. Aug. 1, 2014). To assess whether amendment-based estoppel arises, "[t]he first question . . . is whether an amendment filed in the Patent and Trademark Office ('PTO') has narrowed the literal scope of a claim. If the amendment was not narrowing, then prosecution history estoppel does not apply." *Festo Corp.*, 344 F.3d at 1366. A "patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim." *Pharma Tech Sols., Inc. v. LifeScan, Inc.*, 942 F.3d 1372, 1380 (Fed. Cir. 2019).

Intel argues that VLSI triggered amendment-based prosecution history estoppel when it amended the '759 patent claims to disclose "the first master device" in generating a request rather than "at least one master device" or "at least one of the plurality of master devices." ECF No. 593 at 11. A comparison between the original and amended claim language is shown in the table below:

Rejected Claim 22	**Asserted Claim 14**
at least one master device coupled to the bus, … wherein ***the at least one*** master device provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency	***a*** first master device coupled to the bus, ***the*** first master device configured to provide a request to change a clock frequency of a highspeed clock in response to a predefined change in performance of ***the*** first master device
Rejected Claim 1	**Issued Claim 1**
monitoring a plurality of master devices coupled to a bus within a system; receiving an	monitoring a plurality of master devices coupled to a bus; receiving a request, from ***a***

input from ***at least one of the plurality*** of master devices, wherein the input is to request an increase to the clock frequency of the bus	first master device of the plurality of master devices,

According to Intel, VLSI's decision to amend the claim in response to the Examiner's express confirmation that such an amendment necessarily refers to "only one master device" creates a presumption that the narrowing relates to patentability. *Id.* at 12. Intel contends that VLSI sought to cover subject matter surrendered by amendment when it alleged that Intel infringed under the doctrine of equivalents based on a theory that the "request" was a "calculated speed change" in combination with an entirely different device. *Id.* at 13.

VLSI argues two reasons as to why the September 10, 2008, amendment was not narrowing. First, the word "alone" never appears in any of the claims. ECF No. 607 at 7. Second, VLSI argues that the indefinite article "a" itself means "at least one" and, consequently, has no impact on the claim's scope. ECF No. 607 at 1 (citing *Crystal Semiconductor v. Tritech Microelectronics*, 246 F. 3d 1336, 1347 (Fed. Cir. 2001). Further, VLSI notes that "[t]he subsequent use of definite articles 'the' or 'said' in a claim to refer back to the same claim term does not change the general plural rule, but simply reinvokes that non-singular meaning." ECF No. 607 at 7 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008)). Thus, the claim does not require that "the first master device" alone generate the request. VLSI asserts that the Examiner did not confirm a change in patent scope; instead, the Examiner pointed out an antecedent basis "informality" as described in the Office Action, which VLSI subsequently cured. *Id.* at 8. VLSI argues that this correction cannot serve as a basis for estoppel and notes that "if the amendment was not narrowing, then prosecution history estoppel does not apply." ECF No. 607 at 6 (citing *Festo Corp.*, 344 F.3d at 1366).

In its Reply, Intel argues that "a" can mean "one" "where the language of the claims . . . or the prosecution history necessitate[s]." ECF No. 616 at 1 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008)). Intel claims this is a case where the prosecution history through the amendment shows an intent to have "a" mean "one." *Id.* Relying on *Laitram Corp. v. NEC Corp.*, Intel argues that any amendment following a rejected claim scope must be a substantive change. 163 F.3d 1342, 1348 (Fed. Cir. 1998) (stating it is "difficult to conceive of many situations in which the scope of a rejected claim that became allowable when amended is not substantively changed by the amendment"). Finally, Intel argues that the Examiner's no antecedent basis rejection must have constituted claim narrowing because the rejection makes no sense under VLSI's theory that "a master device" means the same thing as "at least one master device." *Id.* If VLSI's theory was correct, Intel posits that the earlier appearing "a master device" language would have provided an antecedent basis for the "at least one master device" limitation. *Id.*

The Court finds that amendment-based estoppel does not apply. The 2008 amendment did not cause a substantive change in the claim language. The Applicant's change did not impact the claim scope because the Federal Circuit has long held that the indefinite article "a" means "at least one." *Crystal Semiconductor*, 246 F. 3d at 1347. In *Crystal Semiconductor*, the Court explained that "[t]his court has consistently emphasized that the indefinite articles 'a' or 'an,' when used in a patent claim, mean 'one or more' in claims containing open-ended transitional phrases such as 'comprising.' . . . . 'Under this conventional rule, the claim limitation 'a,' without more, requires at least one.'" *Id.* The amendment was not a substantive change and did not transform the meaning of the claim to somehow mean "the first master device' *alone* to generate the 'request'". Without any reference to "alone" in any of the claims, this Court will not reinterpret the Federal Circuit's

instruction that "a" means "at least one." Moreover, the Examiner's characterization of the rejection as an informality indicates a non-substantive impact on patentability. If the Examiner understood that curing the informality would materially change the patent claim's scope, it likely would not have described the rejection as such. Moreover, although "a" can mean "one" where the prosecution history necessitates such an interpretation, the prosecution history in this case does not reveal such an interpretation.

Here, the amendment did not narrow the claim scope. Accordingly, VLSI's DOE theory is not barred by amendment-based prosecution history estoppel.

2) VLSI's amendment to '759 patent claims does not trigger the application of argument-based prosecution history estoppel.

Argument-based estoppel arises when an applicant distinguishes prior art through argument (rather than amendment) made during prosecution. *Amgen*, 931 F.3d at 1159. To invoke argument-based estoppel, "the prosecution history must evince a clear and unmistakable surrender of subject matter." *Conoco, Inc. v. Energy & Env't Int'l, L.C.*, 460 F.3d 1349, 1364 (Fed. Cir. 2006). The clear and unmistakable standard is a high bar. *Silt Saver, Inc. v. Hastings*, No. 1:16-CV-1137-SCJ, 2017 U.S. Dist. LEXIS 216827, at *25 (N.D. Ga. Oct. 18, 2017). "The relevant inquiry is whether a competitor would reasonably believe that the applicant had surrendered the relevant subject matter." *Id.* "[T]he determinations concerning whether the presumption of surrender has arisen and whether it has been rebutted are questions of law for the court, not a jury, to decide." *Festo* Corp, 344 F.3d at 1368. The Court "do[es] not presume a patentee's arguments to surrender an entire field of equivalents through simple arguments and explanations to the patent examiner." *Conoco, Inc.*, 460 F.3d at 1364.

Intel asserts that argument-based prosecution history estoppel bars VLSI's equivalents theory because it clearly and unmistakably surrenders any claim that the "request" limitations can

be met in systems where a master device "selects the frequency based on a number of factors." ECF No. 593 at 15. Intel claims that the distinction VLSI drew between its claim and the Ansari reference to overcome a prior art rejection demonstrates that the selection of "frequency based on a number of factors" is not "a master device making a request" and requires that an input do more than "happen to cause" a change to the master device's frequency. *Id.* Consequently, Intel contends that VLSI inappropriately presented an equivalents theory barred by argument-based prosecution history estoppel because the accused Intel products evaluate "various factors" that may "happen to cause" a change in clock speed in deciding whether to change frequency. *Id.* at 16.

VLSI argues that the prosecution history does not evince clear and unmistakable surrender of its DOE theory. ECF No. 607 at 9. VLSI contends that the Intel's argument rests on an entirely different DOE theory than the one VLSI actually presented at trial. *Id.* Specifically, VLSI's theory turned on the combination of components that generate the "request" rather than the "request" itself, as Intel suggests. *Id.* Thus, VLSI claims to have distinguished the '759 Patent from Ansari because the reference disclosed a request from a master device that "happens to cause an arbiter to increase the bus speed" instead of a master device that causes a change in bus speed itself. *Id.* at 10. Further, VLSI argued that Intel's internal documents proved that the Accused Products fell within the scope of the limitation because they disclosed a ratio produced by a combination of components for modifying the clock frequency depending on the core's workload. *Id.* at 11.

The Court looks first to the argument made during prosecution of the '759 Patent. In response to the Examiner's prior art rejections, the Applicant explained that in Ansari a "master device seeking bus resources to initiate a transaction sends a bus request and a destination address to the bus arbiter so that the arbiter can determine a corresponding bus frequency." PTX-8-A.241-.242. The bus request in Ansari is sent by the master device to the arbiter to *access* the bus. *Id.*

Crucially, the "master device does not determine or request a desired bus frequency because it is the bus arbiter that determines the bus frequency based on various factors." *Id.* By contrast, the '759 Patent recites a first master device that provides a request to change the clock frequency of a high-speed clock. '759 Patent 8:52–55. The bus request to an arbiter causing *access* to the bus in Ansari is distinct from the bus request to *increase* the clock frequency in the '759 Patent. Thus, the Applicant distinguished the "request" from Ansari from the "request" in the '759 Patent.

The Court looks next to the DOE theory that VLSI presented at trial. Dr. Conte, VLSI's expert, testified to VLSI's infringement theory at trial. He explained that the core and its associated code in the programmable clock controller generate the "request." Sealed Trial Tr. 55:1-6; 53:14-56:3; ECF No. 553-02 PDX4.204-214. Intel mischaracterizes his testimony as a DOE opinion based on the claimed "request." Dr. Conte testified as to how the combination of the core ("first master device") and its code in the programmable clock controller ("PCU") provide the request. ECF No. 607 at 10. Specifically, Dr. Conte explained that the core sends Core_Active signals to the PCU [redacted] 39:23-40:7; PTX-1805; *see also* Sealed Trial Tr. 42:13-43:4; ECF No. 553-02 PDX4.171-172. The PCU's "C0 residency counters" then measure the activity of the core, and those counters start counting when the core sends the Core_Active signal to the PCU. Trial Tr. 1419:2-18; ECF No. 553-03 PDX5.13. [redacted] the "P-Code" in the PCU sends a request for a higher or lower frequency. PTX-3484.3. [redacted] 553-02 PDX4.207; D-1154. Although the literal infringement opinion was based on the Core_Active signals, the DOE theory was predicated on the combination of the core's output and the P-Code. PTX-3484.3. Dr. Conte also supported his DOE opinion using the "function, way, result" test. Sealed Trial Tr., 55:1-6; ECF No. 553-02 PDX4.202. He explained that the difference

between Intel's products and the '759 Patent is "just a difference of where an engineer draws this [dotted] line . . . a design choice." Sealed Trial Tr., 55:12-17; ECF No. 553-02 PDX4.207, -.209.

Having reviewed the argument to the Examiner and the DOE theory presented at trial, the Court finds that argument-based estoppel does not apply. VLSI's conduct fails to rise to the level of a "clear and unmistakable surrender of subject matter." First, VLSI's DOE theory is sufficiently distinct from the arguments the Applicant made to the Examiner in distinguishing Ansari. The Applicant did not argue that that master device and arbiter together provide a request to change the clock frequency. Rather, the Applicant argued that the master device sends a bus request to the arbiter in order to access the bus. Nothing in the Applicant's argument disclaimed the idea that the core and its associated P-Code in the PCU could provide the request. VLSI's DOE theory turned on the components that provide the request in Intel's accused products, not the request itself, as Intel suggests. Second, even if Intel is correct that the Applicant's argument encompassed VLSI's DOE theory, there is simply not enough evidence of "clear and unmistakable surrender" of VLSI's DOE theory. Intel has failed to meet this high bar. Thus, this Court will not prevent VLSI from relying on its DOE theory on the ground of argument-based prosecution history estoppel.

B. The ensnarement doctrine does not bar VLSI's doctrine of equivalents theory.

"Ensnarement bars a patentee from asserting a scope of equivalency that would encompass, or 'ensnare,' the prior art." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1322 (Fed. Cir. 2009). That is, "there can be no infringement if the asserted scope of equivalency of what is literally claimed would encompass the prior art." *Wilson Sporting Goods Co. v. David Geoffrey & Assocs.*, 904 F.2d 677, 683 (Fed. Cir. 1990). Whether a proposed equivalent ensnares prior art is typically based on a "hypothetical claim analysis," which puts the burden on the patentee to identify a hypothetical claim that contains both the literal claim scope and the proposed

equivalent without ensnaring the prior art. *Intendis GMBH v. Glenmark Pharms. Inc.*, 822 F. 3d 1355, 1363 (Fed. Cir. 2016). However, a "hypothetical claim analysis is not the only method in which a district court can assess whether a doctrine of equivalents theory ensnares the prior art." *G. David Jang, M.D. v. Box. Sci. Corp.*, 872 F.3d 1275, 1285, n.4. (Fed. Cir. 2017). In the context of a hypothetical claim analysis, "[t]he burden of producing evidence of prior art to challenge a hypothetical claim rests with an accused infringer, but the burden of proving patentability of the hypothetical claim rests with the patentee." *Interactive Pictures Corp. v. Infinite Pictures, Inc.*, 274 F.3d 1371, 1380 (Fed. Cir. 2001)

As a preliminary matter, the parties dispute whether VLSI proposed a hypothetical claim and whether that disclosure was timely. Intel argues that the ensnarement doctrine bars VLSI's equivalents theory for the '759 Patent because VLSI failed to propose a hypothetical claim that does not ensnare the prior art. ECF No. 593 at 18. To suggest that the burden lies on VLSI to assert the defense, Intel points to a Northern District of California case stating that "(1) because the patent holder was on notice of the asserted ensnarement defense, the patent holder 'must articulate an adequate hypothetical claim'" as "a necessary step in the [doctrine of equivalents] infringement theory," and (2) by failing to take "this necessary step in its infringement theory, . . . patent owner too disclaims the theory." *Id.* at 19 (citing *Fluidigm Corp. v. IONpath, Inc.*, No. C 19-05639 WHA, 2021 WL 292033 (N.D. Cal. Jan. 28, 2021)). Intel proposes that the same outcome should apply to this case given that it notified VLSI of an ensnarement defense over a year before filing this motion. *Id.*

In response, VLSI notes that a hypothetical claim analysis is not required in assessing whether a DOE theory ensnares the prior art. ECF No. 607 at 13. Still, VLSI asserts that it did propose a hypothetical claim implicitly through Dr. Conte's testimony. *Id.* at 14. Specifically, Dr.

Conte testified that the accused products triggered application of DOE "by using the combination of a core and the PCU to provide a request" to modify a clock frequency. *Id.* VLSI asserts that Dr. Conte's testimony illustrated how the "request" limitation did not ensnare the prior art and provided Intel notice of a hypothetical claim supporting VSLI's DOE theory. *Id.* When a hypothetical claim is proposed, the accused infringer has the burden to challenge it. VLSI argues that although Intel referred to certain alleged prior art, it failed to provide a detailed analysis satisfying its affirmative burden of production. *Id.*

The Court finds that a hypothetical claim was not required for this Court to determine whether VLSI's DOE theory ensnares the prior art. *Jang*, 872 F.3d at 1285, n.4; see also *Conroy v. Reebok Int'l, Ltd.*, 14 F.3d 1570, 1577 (Fed. Cir. 1994) ("While the hypothetical claim analysis is a useful methodology because the clear step-by-step process facilitates appellate review, nothing in *Wilson* mandates its use as the only means for determining the extent to which the prior art restricts the scope of equivalency that the party alleging infringement under the doctrine of equivalents can assert."). Still, the Court notes that VLSI asserted a hypothetical claim, and its disclosure was timely. The parties in this case expressly agreed to defer for submission any proposed findings of fact and conclusions of law relating to Intel's ensnarement defense. ECF No. 398-02. In fact, it is commonplace for courts to accept hypothetical claims after a jury has rendered a verdict. *See Jang*, 872 F.3d at 1285 (district court considered hypothetical claims proposed by plaintiff for the first time in a post-verdict hearing). VLSI's hypothetical claim in its proposed findings of fact is thus timely. Intel nevertheless claims to have suffered prejudice from this post-verdict disclosure, but this Court finds that Intel had sufficient notice of VLSI's hypothetical claim. Dr. Conte's testimony that the accused products invoked the doctrine of equivalents "by using a combination of a core and the PCU to provide the request" to modify a clock frequency was

sufficiently detailed to provide timely notice to Intel of VLSI's DOE theory. Intel had time to take discovery on this issue and could have challenged the DOE theory during Dr. Conte's deposition. Any arguments about untimeliness and prejudice are unpersuasive.

Notwithstanding the lack of a hard-and-fast requirement for a hypothetical claim analysis, VLSI contends that its hypothetical claim is also patentable in view of the Terrell, Ansari, and Yonah references. ECF No. 607 at 15–17. VLSI's proposed hypothetical claim, which corresponds to claim 14 of the '759 Patent, is below:

> Hypothetical Claim. A system comprising: a bus capable of operation at a variable clock frequency; a first master device coupled to the bus, the first master device or the first master device and its associated code in a programmable clock controller configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and the ~~a~~ programmable clock controller having an embedded computer program therein, the computer program including instructions to: receive the request provided by the first master device or the first master device and its associated code in the programmable clock controller; provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller; and provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller.

Intel contends that VLSI's hypothetical claim improperly ensnares prior art for four reasons. ECF No. 616 at 8. First, Intel alleges that VLSI's hypothetical claim fails to cover the full scope of its equivalents theory because it provides periodically sampled data continuously, not "in response to a predefined change in performance." *Id.* Second, Intel claims that VLSI failed to address several prior art references Intel identified as ensnared prior art during discovery. *Id.* Third, Intel states that VLSI improperly alleges that the Terrell reference does not expressly disclose a

requirement for teaching a system bus. *Id.* Lastly, Intel argues that VLSI's hypothetical claim ensnares the Ansari reference when combined with Terrell. *Id.*

It is unclear whether Intel has met its burden in producing prior art to challenge the hypothetical claim. Its Motion focuses on the timeliness of disclosure and prejudice, and its Reply devotes only one and a half pages to the hypothetical claim analysis. Still, the Federal Circuit has indicated this is a burden of production, and Intel at the very least has produced, albeit through vague citations, three references that this Court will consider—Terrell, Ansari, and Yonah. VLSI has the burden to prove that the hypothetical claim is patentable.

VLSI first argues that the hypothetical claim is patentable over Terrell, alone or in combination. ECF No. 607 at 16. Several elements of the hypothetical claim are lacking in Terrell. Among these include the fact that Terrell does not teach the limitation of providing the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus. Dr. Conte testified that Terrell lacks this element of controlling the clock frequency of the bus, and Intel's expert, Dr. Dirk Grunwald, admitted that Terrell does not teach this limitation. ECF No. 608-3 ¶ 515. Without that limitation, the hypothetical claim cannot encompass Terrell.

VLSI next argues that the hypothetical claim is patentable over Ansari. *Id.* at 16–17. There are at least three distinctions between the hypothetical claim and Ansari. As explained above, Ansari discloses a master device that makes a request to the bus arbiter to access the bus. ECF No. 608-3. The hypothetical claim, by contrast, recites "the first master device or the first master device and its associated code in a programmable clock controller configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device." The hypothetical claim does not request access, but rather requests an increase in clock frequency of a high-speed clock or the bus. Another distinction is that the Ansari

master device makes a request to access the bus and does not make request "in response to a predefined change in performance." ECF 608-4, col. 11:4–9. By contrast, the hypothetical claim discloses a request that is provided "in response to a predefined change in performance." Both of those distinctions were made by the Applicant during the prosecution of the '759 Patent. ECF No. 607. Lastly, the hypothetical claim recites "provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request." PTX-5, col. 8:63-67 (claim 14); *see also* col. 9:26-30 (claim 18). Ansari does not disclose this controlling the clock frequency of a second master device in response to receiving a request from the first master device. ECF No. 607 at 17.

VLSI also argues that the hypothetical claim is patentable over Yonah. ECF No. 607 at 17–18. The Yonah processor was discussed at trial. When questioned about Yonah, Dr. Conte testified that the Yonah processor did not have "a programmable clock controller having an embedded computer program therein, the computer program including instructions to: receive the request . . . ; provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus . . . ; and provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus." Trial Tr. [Conte] 1410:12-20; *see also* Trial Tr. 1412:17-1417:20. By contrast, the hypothetical claim recites this programmable clock controller with an embedded program that includes instructions. At trial, the jury found that Yonah did not anticipate the claims of the '759 Patent. ECF No. 564 at 6.

This Court finds that neither of the three prior art relied on by Intel ensnare Dr. Conte's DOE infringement analysis. First, the disclosed limitation does not ensnare Ansari. One such distinction is that the master device in Ansari makes a request to the bus arbiter to *access* the bus 620 to initiate a transaction, but the master device in the hypothetical claim makes a request to

increase clock frequency of a high-speed clock or the bus. Similarly, Terrell fails to teach controlling the clock frequency of the high-speed clock in the hypothetical claim. Lastly, Yonah lacks the programmable clock controller that is recited in the hypothetical claim. VLSI has met its burden to show that its hypothetical claim is patentable over the prior art. Therefore, this Court holds that VLSI's equivalents theory does not ensnare the prior art.

C. The claim vitiation doctrine does not bar VLSI's doctrine of equivalents theory.

Another limit on the doctrine of equivalents is the "all elements" rule. Under the doctrine of equivalents, "the range of equivalents cannot be divorced from the scope of the claims." *Vehicular Techs. Corp. v. Titan Wheel Int'l, Inc.*, 212 F.3d 1377, 1382 (Fed. Cir. 2000). "[I]f a theory of equivalence would entirely vitiate a particular claim element, partial or complete judgment should be rendered by the court . . . ." *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 39 n. 8 (1997). The "all elements" rule precludes using the doctrine of equivalents when "a limitation would be read completely out of the claim—i.e., the limitation would be effectively removed or 'vitiated.'" *DePuy Spine*, 469 F.3d at 1017.

Intel's final argument is that VLSI's proposed equivalent improperly vitiates the requirements of the asserted claims under the "all elements" rule. ECF No. 593 at 19. According to Intel, the claim requires not only providing the "request" but also specifies that the request should be generated "in response to a predefined change in performance of the first master device." *Id.* at 20. But Dr. Conte testified that its proposed equivalent, C0 residency data, is sent without regard to a change in performance, not in response to a change in performance. *Id.* Because VLSI's expert agreed that C0 residency data is not the claimed "request," Intel argues that any equivalents theory based on such data must fail. *Id.* Intel argues that such a reading would vitiate the claim

requirement that "requests" are sent "in response to a predefined change in performance of the first master device." *Id.*

There are two problems with Intel's claim vitiation argument. First, Intel mischaracterizes the law. Claim vitiation "is not an exception or threshold determination that forecloses resort to the doctrine of equivalents, but is instead a legal conclusion of a lack of equivalence based on the evidence presented and the theory of equivalence asserted." *Bio-Rad Lab'ys, Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1366–67 (Fed. Cir. 2020). At its core, claim vitiation is a conclusion that "no reasonable jury could conclude that an element of an accused device is equivalent to an element called for in the claim, or that the theory of equivalence to support the conclusion of infringement otherwise lacks legal sufficiency." *DePuy Spine*, 469 F.3d at 1018–19. Intel's claim vitiation arguments attempt to substitute de novo review for substantial evidence review, which places a heavy burden on Intel to prove that the jury's verdict is not supported by substantial evidence. Intel has failed to meet that burden. Intel presents no compelling reason to believe that substantial evidence did not support the jury's verdict.

Second, Intel's claim vitiation argument mischaracterizes VLSI's expert testimony. Contrary to Intel's assertion, Dr. Conte did not opine that C0 residency counters are "requests." Rather, he explained that the C0 residency counters count how long the Core_Active signal from the core is active. Trial Tr. 1419:2-18; ECF No. 553-03 PDX5.13. [redacted], then the combination of the P-Code in the PCU and the core (which sends the Core_Active signals) produce the "request" for a change in frequency. Sealed Trial Tr., 56:7-57:7; D-1154. In sum, Dr. Conte's testimony established that under the doctrine of equivalents, (1) the core sends a Core_Active signal in response to a "predefined change in performance" of the core, (2) the Core_Active signal

starts the [redacted], and (3) the output of processing of the Core_Active signals constitutes a "request." ECF No. 607 at 20.

This Court agrees with VLSI that its doctrine of equivalents theory does not read out any claim limitations. The limitations that Intel complains are vitiated are: (1) the requirement to provide the "request" and (2) that the request should be generated "in response to a predefined change in performance of the first master device." First, VLSI's DOE theory includes a requirement to provide a "request" through the combination of the P-Code in the PCU and the output of the Core_Active signals. Second, VLSI's DOE theory does generate a request "in response to a predefined change in performance of the first master device." VLSI proved that the Core_Active signals are sent "whenever the core becomes active." Trial Tr. 488:4-7. Dr. Conte's testimony confirms this: "Q. Are Core_Active signals sent periodically? A. No. Q. When are they sent? A. They're sent whenever the core becomes active." *Id.* Intel cherry picks Dr. Conte's testimony about periodic signals and Core_Active signals to try and reshape VLSI's DOE theory into something it is not. Accordingly, this Court holds that claim vitiation under the "all elements" rule does not apply to VLSI's DOE theory.

IV. CONCLUSION

This Court finds that prosecution history estoppel, the ensnarement doctrine, and claim vitiation do not preclude VLSI's DOE theory. Therefore, Intel's Motion for Judgment of No Infringement of the '759 Patent Under the Doctrine of Equivalents is **DENIED**.

SIGNED this 18th day of March, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff*	§	
	§	
	§	**6:21-CV-57-ADA**
-v-	§	
	§	
INTEL CORPORATION, *Defendant*	§	
	§	
	§	
	§	

ORDER DENYING LEAVE TO AMEND (ECF No. 349)

Before the Court is Defendant Intel Corporation's ("Intel") Motion for Leave to Amend Answer, Defenses, and Counterclaims and to Sever and Stay Defense of License. ECF No. 349. Plaintiff VLSI Technology LLC ("VLSI") filed its Response on November 30, 2020. ECF No. 371. For the reasons described herein, the Court **DENIES** Intel's Motion.

I. BACKGROUND

Plaintiff VLSI filed its suit for patent infringement on April 11, 2019. ECF No. 1. VLSI accused Intel of infringing U.S. Patent Nos. 7,523,373 ("the '373 Patent") and 7,725,759 ("the '759 Patent"). The Court held a jury trial, which concluded on March 2, 2021, with a verdict in VLSI's favor. ECF No. 556. The jury found that Intel literally infringed on the '373 Patent and that Intel infringed on the '759 Patent only under the doctrine of equivalents ("DOE"). ECF No. 593 at 1. The jury awarded over $2 billion in damages to VLSI.

VLSI is a subsidiary of CF VLSI Holdings LLC, a Delaware limited liability company. ECF No. 195-2 ¶ 7. CF VLSI Holdings LLC is owned by ten separate entities, which in turn are owned by pension funds and third-party investors. *Id.* Those pension funds are managed by

Fortress Investment Group LLC ("Fortress"). *Id.* ¶ 10. VLSI's CEO stated that Fortress does not own VLSI. *Id.*

In June 2020, Fortress acquired Finjan, Inc. and executed the Finjan Merger Agreement, which states that the parties to the agreement are Finjan Holdings, Inc., CFIP Goldfish Holdings LLC, and CFIP Goldfish Merger Sub Inc. ECF No. 195-2. Fortress Credit Opportunities Fund V (A) L.P. and Fortress Intellectual Property Fund I (A) LP are described in the Finjan Merger Agreement as equity financing sources for the two Goldfish entities. *Id.*

Intel alleges that it obtained a license to all the Asserted Patents. ECF No. 349 at 1. It claims that it obtained the license pursuant to a November 12, 2012, Settlement Agreement between Intel and Finjan, Inc. and Finjan Software, Inc. (the "Finjan License"). *Id.* Intel contends that Finjan, Inc. and Finjan Software, Inc. are affiliated companies to VLSI because they are now all under the common control of Fortress. *Id.* VLSI denies that it is bound by the license and contends it is a total stranger to the agreement. *Id.*

Intel asserted its affirmative defense of license that was not decided at trial because the Court had not yet ruled on Intel's Motion for Leave to Amend its Counterclaims to add the defense of license. The pleadings at the time of trial did not include the license defense. Intel now asks the Court for leave to amend the pleadings to add its license defense. ECF No. 349 at 1. Alternatively, it asks this Court to sever and stay its affirmative license defense. *Id.* at 2.

II. LEGAL STANDARD

When a party requests leave to amend after a scheduling order's deadline has expired, Rule 16(b) governs the court's analysis, and rule 15(a) is inapplicable. *See Squyres v. Heico Cos., LLC*, 782 F.3d 224, 237 (5th Cir. 2015). Rule 16(b)(4) provides that the contents of a court's scheduling order "may be modified only for good cause and with the judge's consent." Fed. R. Civ. P.

16(b)(4). To determine if good cause exists, the Court should consider "(1) the explanation for the failure to timely comply with the scheduling order; (2) the importance of the modification; (3) potential prejudice in allowing the modification; and (4) the availability of a continuance to cure such prejudice." *Squyres*, 782 F.3d at 237 (citing *Meaux Surface Protection, Inc. v. Fogleman*, 607 F.3d 161, 167 (5th Cir. 2010)).

"[T]he party seeking to modify the scheduling order has the burden of showing 'that the deadlines cannot reasonably be met despite the diligence of the party needing the extension.'" *Id.* (quoting *Filgueira v. US Bank Nat'l Ass'n*, 734 F.3d 420, 422 (5th Cir. 2013) (per curiam)). "Mere inadvertence on the part of the movant and the absence of prejudice to the non-movant are insufficient to establish good cause." *Morris v. Nat'l Seating & Mobility, Inc.*, No. 5-18-CV-00048-FB, 2019 WL 2343020, at *6 (W.D. Tex. June 3, 2019) (internal citations and quotations omitted). In addition, "[a] futile amendment need not be allowed under Rule 16(b)." *Adams Family Trust v. John Hancock Life Ins. Co., U.S.A.*, 424 Fed.Appx. 377 (5th Cir. 2011).

III. DISCUSSION

In its Motion, Intel asks this Court to grant leave to amend the pleadings so it can add a license defense. The deadline to amend pleadings under the scheduling order in this case was March 6, 2020. ECF No. 115. The standard for granting leave to amend the pleadings after a scheduling order deadline has expired is governed by Rule 16(b)(4). *Squyres*, 782 F.3d at 237. Courts analyze four factors in deciding whether good cause exists to allow for modification of the scheduling order. This Court will analyze those four factors below.

A. The four factors that courts consider in granting leave to amend show that Intel's Motion should be denied.

1) Intel fails to provide a good explanation for its failure to timely comply with the scheduling order.

The first factor that a Court will consider in granting leave to amend is the moving party's explanation for a failure to timely comply with the scheduling order. Intel argues that it was impossible to amend its answer before the March 6, 2020, deadline because VLSI became an "Affiliate" of the Finjan parties on July 24, 2020, when Fortress acquired Finjan. ECF No. 349 at 4. VLSI responds that Intel delayed for months to file the motion to amend on November 11, 2020. ECF No. 371 at 3. VLSI also complains that Intel did not notify VLSI of its intent to rely on this defense in this action specifically. *Id.*

Intel's explanation for a failure to timely comply with the scheduling order is unpersuasive. The over three-month gap in between the Finjan Merger Agreement and the filing of this Motion is inexcusable. Not only did Intel allow fact and expert discovery deadlines to pass, it also filed summary judgment and Daubert motions without ever evincing an intent to invoke its license defense. Instead, it brought this Motion at the eleventh hour, just one month before the original pretrial conference date. ECF No. 371 at 3. Intel's late filing of its Motion resembles more of a tactic to delay trial rather than a good faith basis for adding its defense.

2) The proposed amendment would be futile because VLSI is not a party to the agreement.

The second factor that Courts consider is the importance of the proposed modification. Intel contends that the amendment would be important because an affirmative defense of license would release it from all liability. Indeed, a license is a valid defense to infringement. *Crossroads Sys. v. Dot Hill Sys. Corp.*, 48 F. Supp. 3d 984, 989 (W.D. Tex. Sep. 19, 2014). Intel cites several cases for the proposition that VLSI is still bound by the agreement despite not being a signatory. ECF No. 349 at 4–5 (citing *Oyster Optics, LLC v. Infinera Corp.*, 2019 WL 2603173, at *6-7, *9-

10 (E.D. Tex. June 25, 2019); *Medtronic AVE v. Cordis Corp.,* 100 F. App'x 865, 867 (3d Cir. 2004); *Medtronic AVE v. Cordis Corp.*, 280 F. Supp. 2d 339, 342 (D. Del. 2003). But Intel's reliance on these three cases is misguided.

First, the Court in *Oyster Optics* found that the defendant held a license to the asserted patents despite not being a signatory to a settlement agreement. *Oyster Optics*, 2019 WL 2603173, at *6-7, *9-10. The defendant was bound by the agreement because a former co-defendant (the signatory to the agreement) in the litigation had acquired the defendant after its settlement with the plaintiff. *Id.* But a critical fact is that the party that granted the license was also the party against whom the license defense was asserted, meaning that it was undisputed that the plaintiff was bound by the agreement. *Id.* at *1. By contrast, VLSI did not grant the license and argues it is not bound by the settlement and license with Finjan because "is not a party to it, never agreed to be bound by it, is not asserting Finjan's patents, and is not owned by Finjan." ECF No. 371 at 6.

Second, in *Medtronic AVE v. Cordis*, the Third Circuit bound an affiliate to an arbitration provision in a patent license that was acquired after the license was made. *Medtronic AVE,* 100 F. App'x at 867. But like the distinction in *Oyster Optics*, the plaintiff in *Medtronic AVE* did not dispute that it was bound by the license agreement. *Id.* at 867–68. VLSI, however, argues that it is not a party to the Finjan License. While the plaintiff in *Medtronic AVE* was a subsidiary of the parent-signatory, VLSI has no relationship to Finjan whatsoever. The same is true of Intel's citation to the District of Delaware *Medtronic AVE v. Cordis Corp.*, case. In that case, there was no dispute that the plaintiff was the affiliate of the parent-signatory under the agreement. *Medtronic AVE*, 280 F. Supp. 2d at 341. Those facts are not present here.

Having distinguished the facts of this case with Intel's cited case law, the Court now turns to the Finjan Merger Agreement and VLSI's corporate structure to determine if it could be bound

by the Finjan License, thus making this defense important to the case. As explained above, VLSI is a subsidiary of CF VLSI Holdings LLC, which in turn is owned by ten separate entities. ECF No. 195-2 ¶ 7. Those entities are owned by pension funds and third-party investors. *Id.* Those pension funds are managed by Fortress. *Id.* ¶ 10. VLSI's CEO stated that Fortress does not own VLSI, but rather "provides administrative services to VLSI in Fortress's capacity as investment advisors to the owners of the company." *Id.*

In June 2020, Fortress acquired Finjan and executed the Finjan Merger Agreement, which states that the parties to the agreement are Finjan Holdings, Inc., CFIP Goldfish Holdings LLC, and CFIP Goldfish Merger Sub Inc. ECF No. 195-2. Fortress Credit Opportunities Fund V (A) L.P. and Fortress Intellectual Property Fund I (A) LP are described in the Finjan Merger Agreement as equity financing sources for the two Goldfish entities. *Id.* Notably, none of the parties to that agreement are among the entities that own VLSI's parent. ECF No. 371 at 1.

The Finjan License provides that all disputes relating to the agreement are governed by Delaware law. ECF No. 188-1 at 13. As VLSI notes, Delaware law provides that a non-party to a contract is not bound by that contract. *Sheehan v. Assured Partners, Inc.*, C.A. No. 2019-0333-AML, 2020 WL 2838575 (Del. Ch. May 29, 2020); *Alliance Data Sys. Corp. v. Blackstone Cap. Partners V L.P.*, 963 A.2d 746 (Del. Ch. 2009). This is true even when the non-party is a close corporate affiliate of the signatory. *Wenske v. Blue Bell Creameries, Inc.*, 2018 WL 5994971, at *3-8 (Del. Ch. Nov. 13, 2018) (parent company not liable for contract entered into by wholly-owned subsidiary); *Kuroda v. SPJS Holdings, LLC*, C.A. No. 4030-CC, 2010 WL 4880659, at *3-8 (Del. Ch. Nov. 30, 2010) (arbitration clause not binding on non-signatory affiliate).

The case law and the Finjan Settlement make clear that VLSI is not bound by the Finjan License with Intel. VLSI was not a party to the Finjan License and it is not an affiliate of Finjan.

The relationship between VLSI and Finjan via Fortress, who maintains a de minimis ownership in VLSI, is tenuous at best. Finjan did not own the asserted patents at the time of the Finjan License, meaning it could not have licensed something it did not own. Thus, the asserted patens in this case could not have been licensed to Intel. Accordingly, allowing Intel to amend to add a defense of license would be futile.

3) The potential prejudice in allowing the amendment is low.

The third factor that courts consider is the potential prejudice that would result in allowing the modification. Intel contends that an amended pleading would not prejudice VLSI because Fortress chose to acquire Finjan, and VLSI was on notice of the license defense on August 17, 2020. ECF No. 349 at 5. Intel also claims that any prejudice to VLSI is outweighed by the prejudice Intel would suffer if it were deprived of the defense. *Id.* VLSI complains that it would suffer prejudice from a lengthy stay in entry of judgment. ECF No. 371 at 8. That in turn would hinder VLSI's ability to license its patents to others, thus stalling VLSI's business. *Id.* at 9.

Allowing an amendment would likely prejudice VLSI. Trial in this case has already occurred, with a jury finding infringement of the asserted patents. The proposed amendment would only further delay entry of judgment, which would prejudice VLSI's ability to license its patents. And prejudice to Intel is likely minimal because it has a remedy outside of this litigation as it can pursue of a breach of contract claim against Finjan. Assuming its claim is true, Intel could obtain money damages from Finjan to be made whole. But this Court finds that prejudice to Intel is unlikely because, as explained above, VLSI is not bound by the Finjan License.

4) The availability of a continuance is irrelevant.

Finally, courts consider the availability of a continuance to cure such prejudice in deciding whether to grant leave to amend. Intel argues that the amendment would not require a continuance

because Intel is moving to sever and stay the license defense. ECF No. 349 at 6. Because Intel is not seeking a continuance, and because the Court has already held a jury trial on the asserted patents, the Court does not consider this factor relevant in its analysis.

B. A severance and stay of the license defense is now moot.

In addition to asking this Court to amend the pleadings, Intel asks this Court to sever its affirmative license defense and to stay adjudication of that defense while this case proceeds to trial and while Intel pursues its license defense in Delaware Chancery Court. ECF No. 349 at 2. Intel's argument for severance and stay is now moot. First, this Court already conducted a jury trial on the Asserted Patents. Second, since the filing of this Motion, the court in Delaware already resolved Intel's license dispute. ECF No. 648-1, Ex. A. On September 30, 2021, Vice Chancellor Zurn issued a ruling that granted in material part the defendants' motions to dismiss Intel's complaint. *Id.* Vice Chancellor Zurn dismissed Intel's claims for declaratory relief and specific performance for a lack of jurisdiction; dismissed Intel's tortious interference claim on the merits; and stayed Intel's breach of contract claims until the license issued is adjudicated in other courts where Intel asserted that defense. *Id*. Accordingly, Intel's request to delay the entry of judgment in this action until the Delaware court rules on the defense is now moot.

IV. CONCLUSION

For the foregoing reasons, Intel has failed to show that good cause exists for this Court to allow Intel to amend the pleadings in this case to add a license defense. Additionally, this Court will not allow a severance and stay of the proceedings, in part because the Delaware Chancery Court has already ruled on that issue. **IT IS ORDERED** that Intel's Motion for Leave to File Amended Answer, Defenses, and Counterclaims and to Sever and Stay Defense of License (ECF No. 349) is **DENIED**.

SIGNED this 18th day of March, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff,*	§	
	§	
	§	**CIVIL NO. 6:21-CV-057-ADA**
v.	§	
	§	
INTEL CORPORATION, *Defendant.*	§	
	§	

ORDER DENYING DEFENDANT INTEL'S RULE 50(B) MOTION FOR JUDGMENT AS A MATTER OF LAW

Before the Court is Defendant Intel Corporation's ("Intel") Rule 50(b) Motion for Judgement as a Matter of Law ("JMOL"). ECF No. 591. Plaintiff VLSI Technology LLC ("VLSI") filed its Response on May 7, 2021. ECF No. 603. Intel then filed its Reply on May 21, 2021. ECF No. 615. Intel asks this Court for a judgment of no infringement for U.S. Patent Nos. 7,523,373 and 7,725,759, a judgment of invalidity for the asserted claims of the '759 patent, and a judgment of no damages. *Id.* After considering the parties' briefs and relevant law, the Court **DENIES** Defendant's Motion on all counts for the reasons below.

I. BACKGROUND

VLSI filed its suit for patent infringement on April 11, 2019. ECF No. 1 at 1. In its Complaint, VLSI accused Intel Corporation ("Intel") of infringing U.S. Patent Nos. 7,523,373 ("the '373 Patent"), and 7,725,759 ("the '759 Patent"). On March 2, 2021, following a six-day trial, the jury found that Intel literally infringed claims 1, 5, 6, 9, and 11 of the '373 Patent, and infringed claims 14, 17, 18, and 24 of the '759 patent under the doctrine of equivalents. ECF No. 564 at 2–3. The jury also found that Intel had not met its burden to prove that claims 14, 17, 18, and 24 of the '759 patent were invalid. *Id.* at 5. The jury awarded VLSI a total of $2.175 billion in

damages: a $1.5 billion lump sum for infringement of the '373 patent and a lump sum of $675 million for infringement of the '759 patent. *Id.* at 6–7. Intel subsequently filed a Rule 50(b) Motion for JMOL on April 9, 2021. ECF No. 591.

II. LEGAL STANDARD

A court may grant JMOL against a prevailing party only if a reasonable jury would not have a legally sufficient evidentiary basis to find for the non-moving party on that issue. Fed. R. Civ. P. 50(a)(1). In deciding a renewed JMOL motion, a "court must draw all reasonable inferences in favor of the nonmoving party, and it may not make credibility determinations or weigh the evidence." *Taylor-Travis v. Jackson State University*, 984 F.3d 1107, 1112 (5th Cir. 2021). The court must disregard all evidence favorable to the moving party that the jury is not required to believe. *Id*. This is because "[c]redibility determinations, the weighing of the evidence, and the drawing of legitimate inferences from the facts are jury functions, not those of a judge." *Wellogix, Inc. v. Accenture, L.L.P.*, 716 F.3d 867, 874 (5th Cir. 2013).

Courts grant JMOL for the party bearing the burden of proof only in extreme cases, when the party bearing the burden of proof has established its case by evidence that the jury would not be at liberty to disbelieve, and the only reasonable conclusion is in its favor. *Mentor H/S, Inc. v. Medical Device Alliance, Inc.*, 244 F.3d 1365, 1375 (Fed. Cir. 2001). JMOL is inappropriate if the record evidence is such that reasonable and fair-minded men in the exercise of impartial judgment might reach different conclusions. *Laxton v. Gap Inc.*, 333 F.3d 572, 579 (5th Cir. 2003).

A jury verdict must stand unless there is a lack of substantial evidence, in the light most favorable to the successful party, to support the verdict. *Am. Home Assur. Co. v. United Space Alliance, LLC*, 378 F.3d 482, 487 (5th Cir. 2004). Substantial evidence is more than a scintilla, but less than a preponderance. *Nichols v. Reliance Standard Life Ins. Co.*, 924 F.3d 802, 808 (5th Cir.

2019). Thus, JMOL must be denied if a jury's verdict is supported by legally sufficient evidence that amounts to more than a mere scintilla. *Laxton*, 333 F.3d at 585.

III. DISCUSSION

I. Substantial Evidence Supports the Jury's Infringement Findings for the '373 and '759 Patents.

The jury found that the C6 SRAM power multiplexer in Intel's accused products literally infringed the '373 patent. It also found that the Speed Shift feature in Intel's accused products infringed the '759 patent under the doctrine of equivalents. Intel seeks JMOL on those findings.

A. Substantial Evidence Supports the Jury's Infringement Verdict For the '373 Patent.

1. Substantial Evidence Supports the Jury's Infringement Finding for The "Minimum Operating Voltage" Limitations.

The asserted method claims of the '373 Patent require "storing the value of the minimum operating voltage" of a memory. '373 Patent 13:13–14. The asserted apparatus claims require "a memory location that stores a value representative of the minimum operating voltage." *Id.* at 13:63–64. The jury found that the C6 SRAM power multiplexer in Intel's Haswell and Broadwell products infringe on claims 1, 5, 6, 9, and 11 of the '373 Patent. ECF No. 591 at 2. At trial, VLSI identified the accused "memory" as the C6 SRAM in Intel's products and the accused "value of the minimum operating voltage" as being stored in Intel's RING_RETENTION_VOLTAGE fuse. *Id.* Intel argues that the accused products do not store the "minimum operating voltage" and therefore do not infringe on the '373 Patent. *Id.*

The Court first looks to the evidence that VLSI presented at trial to determine whether there is substantial evidence to support the jury's verdict. VLSI argues that it presented substantial evidence that the accused "memory" is the C6 SRAM, and the "minimum operating voltage of the memory" is the RING_RETENTION_VOLTAGE. ECF No. 603 at 1–2. VLSI points to Intel

internal documents that indicate that the [redacted] *Id.* at 2 (citing PTX-3662.702; PTX-3851.1280). Dr. Thomas M. Conte, VLSI's infringement expert, testified that Intel's use of the term "retention" is synonymous with "memory" and that [redacted] applies to C6 SRAM memory. 2/23 Sealed Trial Tr. 5:1-6. He then explained that the RING_RETENTION_VOLTAGE stores the minimum retention voltage for the C6 SRAM. *Id.* at 75:23-76. Dr. Conte further explained that the [redacted] "defines the lowest safe voltage" and thus "the minimum operating voltage." *Id.* at 4:19-25, 9:10-22. VLSI corroborated his testimony with source code in the Haswell and Broadwell products. 3/1 Trial Tr. 1451:4-1452:5.

The Court looks next to Intel's arguments that the above evidence fails to show that its products satisfy the "minimum operating voltage" limitation. According to Intel, RING_RETENTION_VOLTAGE is merely a voltage at which the C6 SRAM *can* retain data, not necessarily the minimum voltage at which data retention occurs as the asserted claims require. ECF No. 591 at 2. Intel contends that Dr. Conte confirmed as much when he admitted that the RING_VF_VOLTAGE_0 fuse value—which is below the RING_RETENTION_VOLTAGE voltage value—reflects a voltage that is "actually used" in the accused products. *Id.* at 5. Because the C6 SRAM, as a ring component, operates at voltages below the RING_RETENTION_VOLTAGE, Intel alleges that no reasonable jury could find that the RING_RETENTION_VOLTAGE fuse stores the C6 SRAM's minimum operating voltage. *Id.* Further, Intel contends that there is no relationship between RING_RETENTION_VOLTAGE and the C6 SRAM *specifically* as opposed to the *entire* ring domain because the voltage applies *generally* to the ring domain, which contains multiple components beyond the C6 SRAM. *Id.*

The first problem with Intel's argument is that it misrepresents Dr. Conte's testimony about the RING_VF_VOLTAGE_0 fuse value. Intel argues that the RING_RETENTION_VOLTAGE cannot store the C6 SRAM's minimum operating voltage because, as Dr. Conte admitted, the accused products "actually use" the RING_VF_VOLTAGE_0 value, which is a lower voltage. ECF No. 591 at 5. But even if the RING_VF_VOLTAGE_0 *fuse* value is below the RING_RETENTION_VOLTAGE *voltage* value, there is still a factual dispute for the jury to resolve as to whether the ring operates at the RING_VF_VOLTAGE_0 *fuse* value. Dr. Conte testified that the ring operates at a higher operating voltage level that is derived from the fuse value after inverse temperature dependence compensations calculations are applied. 3/1 Trial Tr. 1425:1-1432:5, 1434:9-1437:7, 1450:8-1452:12. Dr. Conte explained that Intel's witnesses did not account for the inverse temperature dependence compensations when comparing the RING_VF_VOLTAGE_0 and the RING_RETENTION_VOLTAGE. *Id.* His testimony thus shows that the operating voltage from the RING_VF_VOLTAGE_0 fuse value is higher than the RING_RETENTION_VOLTAGE. This testimony was also corroborated with multiple Intel internal documents. One such example is an Intel specification that shows [redacted] [redacted] *Id.* at 1425:1-1426:20. He came to this conclusion after reviewing Intel's source code for the accused products. *Id.* at 1451:4-1452:5. The jury was free to credit that testimony over Intel's witnesses, particularly after Intel's expert was impeached with Intel documents. ECF No. 603 at 6. As VLSI indicated, Intel's internal documents described RING_RETENTION_VOLTAGE as the [redacted] for "memory", or the C6 SRAM, where the [redacted] is the lowest safe voltage and thus the minimum operating voltage. ECF No. 603 at 2.

The second problem with Intel's argument is that it mischaracterizes the relationship between the RING_RETENTION_VOLTAGE and the C6 SRAM. As VLSI argues, the '373 Patent claims do not recite the word "specifically" to require that the RING_RETENTION_VOLTAGE apply to the C6 SRAM specifically. ECF No. 603 at 2. Nor does the '373 Patent bar the "minimum operating voltage of the memory" from applying to parts in addition to the memory. ECF No. 603 at 2. The patent claims draw no distinction between a specific or general relationship connecting the minimum operating voltage to the C6 SRAM. Instead, the '373 Patent claims include the transition term "comprising", and it is black-letter law that "[t]he transitional term 'comprising' . . . is inclusive or open-ended and does not exclude additional, unrecited elements." *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005). Because RING_RETENTION_VOLTAGE applies to both the "LLC" and C6 SRAM memories, VLSI concludes that RING_RETENTION_VOLTAGE is the minimum operating voltage of the C6 SRAM. *Id.* VLSI presented several sources supporting its claim, including multiple Intel documents and source code reviews. *Id.* at 6. The jury ultimately believed VLSI's expert over Intel's witnesses.

This Court agrees that VLSI has presented substantial evidence supports the jury's infringement finding for the "minimum operating voltage" limitations. VLSI's presentation of Dr. Conte's expert testimony, Intel internal documents, and Dr. Conte's source code analysis provided substantial evidence to support the jury's infringement finding. Although Intel makes several distinct but related arguments that it cannot infringe on this limitation, the Court finds that VLSI presented substantial evidence to the contrary. Intel's arguments fall short of the high bar required for JMOL, which demands a showing that the jury would not be at liberty to disbelieve Intel's non-infringement theory considering the evidence. Instead, Intel's internal documentation and claim

construction argument reinforces the jury's infringement verdict as a reasonable one. Accordingly, this Court denies Intel's motion for JMOL on this ground.

2. Substantial Evidence Supports the Jury's Infringement Finding for the "When" Limitations.

The asserted method claims recite limitations "providing" "as the operating voltage of the memory" (1) "the first regulated voltage . . . when the first regulated voltage is at least the value of the minimum operating voltage," and (2) "the second regulated voltage . . . when the first regulated voltage is less than the value of the minimum operating voltage." '373 Patent 13:20–28, 41–44, 45–52. The asserted apparatus claims also require "a power supply selector that supplies" as the operating voltage of the memory (1) "the first regulated voltage ... when the first regulated voltage is at least the minimum operating voltage" and (2) "the second regulated voltage ... when the first regulated voltage is below the minimum operating voltage." *Id.* at 13:59–14:15, 14:20–23. At trial, VLSI argued that the "first regulated voltage" was Intel's VCCR, the "second regulated voltage" is the VCCIO, and the minimum operating voltage is RING_RETENTION_VOLTAGE.

Intel alleges that VLSI introduced no evidence that the RING_RETENTION_VOLTAGE fuse value is ever used to guide "when" VCCR and VCCIO are supplied. ECF No. 591 at 6. Intel alleges that VLSI ignores the evidence that VCCR is supplied to the C6 SRAM even when VCCR is below RING_RETENTION_VOLTAGE conditions that are the opposite of what the claims require. ECF No. 615 at 4. To avoid confronting this, Intel claims VLSI improperly characterizes the plain meaning of the "when" limitations as an untimely claim construction dispute. *Id.*

VLSI responds that it offered substantial evidence that these limitations are met. Dr. Conte demonstrated that the "first regulated voltage" (VCCR) is supplied when the first regulated voltage is at least the value of RING_RETENTION_VOLTAGE, the minimum operating voltage. 2/23 Sealed Trial Tr. 13:2-16. He explained this using a demonstrative that showed the jury how VCCR

is supplied when it is at least the minimum voltage. PDX4.79. He also confirmed this infringement argument using Intel's documents. 2/23 Sealed Trial Tr. 13:23-14:11.

This Court agrees that VLSI presented sufficient evidence to support the jury's infringement finding. Intel argues VLSI introduced "no evidence" that the RING_RETENTION_VOLTAGE fuse value is ever used to guide "when" the "first regulated voltage" and "second regulated voltage" are supplied ECF No. 591 at 6. Yet Dr. Conte demonstrated that RING_RETENTION_VOLTAGE acts as the threshold for when the voltages are supplied. *Id.* at 7. He supported his testimony with Intel documents, which together provide substantial evidence that Intel met this limitation. Intel rebuts by pointing to an admission by VLSI's expert that he did not refer to RING_RETENTION_VOLTAGE in describing multiplexer operation, but this argument merely introduces a factual dispute. The significance of this dispute is questionable, given that the claims only require that the "first regulated voltage" rise to at least the minimum operating voltage rather than require the minimum operating voltage "to guide." ECF No. 603 at 7. At best, Intel provides evidence of a legitimate factual dispute; at worst, Intel attempts to prevail with a red herring. In either case, Intel petitions this Court to subvert the jury's role by weighing the evidence and making credibility determinations. That is not the Court's task at this stage. See *Wellogix*, 716 F.3d at 874. Accordingly, this Court preserves the jury's verdict and declines JMOL on this ground.

3. Substantial Evidence Supports the Jury's Infringement Finding for The "First Regulated Voltage" And "Functional Circuit" Limitations.

The asserted method claims recite that "while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit." '373 Patent 13:26–28, 41–44, 45–52. The asserted apparatus claims "a power supply

selector" that "supplies the second regulated voltage" to the memory "while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage." *Id.* at 14:8–15, 14:20–23. At trial, VLSI identified Intel's VCCR as the "first regulated voltage" and the VCCIO as the "second regulated voltage." ECF No. 591 at 7.

Intel contends that the functional circuit in its products are not provided with and do not use the first regulated voltage while the second regulated voltage is provided to the memory. *Id.* at 6. Intel's witnesses testified the "first regulated voltage" is actually unregulated and the ring domain components are inoperable during the state in which the "second regulated voltage" powers the C6 SRAM bitcells. *Id.* Moreover, Intel contends that Dr. Conte admitted that the [redacted] *Id.* Thus, Intel alleges that VLSI identifies no evidence supporting its claim that VCCR is regulated during Package C7. *Id.* Intel complains that VLSI's reliance on one Intel document does not account for its engineer's testimony that the "first regulated voltage" is not actually regulated during Package C7. ECF No. 614 at 4. Consequently, Intel asserts JMOL is required because no reasonable jury could find that the "first regulated voltage" is regulated and provided to or used by a "functional circuit" while the "second regulated voltage" is "provided" or "supplied" to what VLSI identifies as the claimed "memory." ECF No. 591 at 8.

To rebut, VLSI cites Dr. Conte's testimony that the "first regulated voltage" is regulated, controlled, and non-zero for the ramp-down period while the "second regulated voltage" is provided to the memory. 2/23 Sealed Trial Tr. 19:16-20:2. Dr. Conte further testified that the circuit is using the voltage and that it is a regulated voltage for the entirety of the Package C7 state. *Id.* VLSI corroborates Dr. Conte's testimony with Intel's internal documents that show that the

[redacted]

see also 2/25 Trial Tr. 870:20–872:25. VLSI argues that Dr. Conte's testimony, coupled with Intel's documents, are substantial evidence that supported the infringement verdict. ECF No. 603 at 8.

This Court agrees with VLSI that substantial evidence supports the jury's infringement finding. JMOL is inappropriate if the record evidence is such that reasonable and fair-minded people in the exercise of impartial judgment might reach different conclusions. *Laxton*, 333 F.3d at 579. Here, Intel presents several points on which expert testimony conflict as to whether the accused products supply a "first regulated voltage" and "second regulated voltage … when the first regulated voltage is below the minimum operating voltage." For example, Intel points out that "the first regulated voltage" is not regulated at all, which directly contradicts Dr. Conte's testimony that the "first regulated voltage" is regulated, controlled, and non-zero. ECF No. 603 at 8. Intel's counters that VLSI lodged an unsubstantiated claim by basing it on an Intel document with no reference to regulation. ECF No. 614 at 4.

This Court's role, however, is not to resolve factual disputes, but to consider whether the evidence mandates non-infringement as the only reasonable conclusion. At best, Intel has demonstrated that there is a legitimate factual dispute over which reasonable minds could differ, rendering JMOL improper. Intel's core contention is that the relevant evidence failed to provide a sound basis for the jury's verdict because it clearly shows, among other things, that the "first regulated voltage" is unregulated. But Intel takes for granted that the jury need only base its verdict on legally sufficient evidence amounting to more than a mere scintilla. The conflicting expert testimonies satisfy that evidentiary standard. Intel's JMOL on this ground is therefore denied.

B. Substantial Evidence Support's The Jury's Doctrine of Equivalents Infringement Verdict for the '759 Patent.

VLSI presented both literal and doctrine of equivalents infringement theories on the '759 patent's "request" limitation. The jury found that the Speed Shift feature in Intel's products infringes multiple claims of the '759 patent under the doctrine of equivalents. Intel argues, however, that JMOL of no infringement should enter because that verdict is contrary to law and not supported by substantial evidence. ECF No. 591 at 8. Intel makes several legal arguments as to why VLSI's doctrine of equivalents claim should be barred. These include prosecution history estoppel and claim vitiation. *Id.* at 9–10. The Court does not address those arguments in this opinion because it already addressed them in its Order denying Intel's Motion for Judgment of No Infringement Under the Doctrine of Equivalents. *See* ECF No. 685. Those arguments are moot. Still, Intel argues that JMOL should be granted because no reasonable juror could have found infringement under the doctrine of equivalents.

In response, VLSI argues that there was substantial evidence sufficient for a reasonable jury to find infringement. ECF No. 603 at 9. But the jury did not find that Intel literally infringed. ECF No. 615 at 5. Whether there was substantial evidence supporting VLSI's rejected claim of literal infringement is irrelevant. To overturn the jury's rejection of its literal infringement claim, VLSI would have had to show that there was no substantial evidence from which a jury could reasonably find non-infringement. *Id.* VLSI has not attempted to meet that burden. *Id.* Therefore, this Court maintains the jury's verdict that the accused products infringe under the doctrine of equivalents and not under literal infringement.

1. Substantial Evidence Supports the Jury's Infringement Finding for the "Request" Limitation.

The '759 Patent relates to the controlling clock frequency in an electronic device. The '759 Patent discloses and claims a system in which a first master device of a plurality of master devices provides a "request" to change a clock frequency of a high-speed clock "in response to a predefined change in performance of the first master device." '759 Patent 7:66–8:15. A "programmable clock controller" receives this "request" and provides outputs to independently control (1) a clock frequency of a second master device coupled to a bus, and (2) a variable clock frequency of the bus. *Id.* VLSI asserted that Intel's Speed Shift feature infringed on claims 14, 17, 18, and 24 of the '759 Patent.

The Court looks first to VLSI's doctrine of equivalents theory and the evidence it used to support its infringement claim. Dr. Conte testified that the combination of core 1 ("first master device") and core 1's associated code in the PCU ("programmable clock controller") provides the claimed "request" in the '759 Patent. Sealed Trial Tr. 55:1-11; 53:14-56:3. Specifically, he explained that the core sends a Core_Active signal to the PCU whenever the core becomes active. Trial Tr. 1419:2-18; 488:4-7. C0 residency counters, which are counters in the PCU, measure the activity of the core over a predefined time interval when the core is active. *Id.* at 1419:12–18. [redacted] generates a "request" for a higher or lower frequency. Sealed Trial Tr., 54:9-22; ECF No. 553-02 PDX4.205-208, PDX4.210. VLSI's literal infringement theory of "request" was based on the Core_Active signals, but its equivalents theory was based on the output of the core in combination with the code in the PCU.

The Court looks next to Intel's arguments that the above evidence fails to show that its products satisfy the "request" limitations. Intel asserts two reasons as to why its products cannot

meet the "request" limitations. ECF No. 591 at 10. First, the C0 residency counters in Intel's products are [redacted] and are not sent "in response to a predefined change in performance" as the claims require. *Id.* Intel claims that Dr. Conte admitted that C0 residency data is [redacted] and [redacted], thus contradicting the claims. *Id.* Second, Intel alleges that VLSI's equivalents theory is inconsistent with the claim, which requires the "request" to be (1) "provided" or "sent" by the "first master device" and (2) "received" by the "clock controller." *Id.* Dr. Conte testified that the "request" in Intel's products is provided by the combination of core and its associated P-code in the PCU ("the first master device"). *Id.* at 11. But Intel argues that this is improper because the claims do not allow the same component to both provide and receive the request. *Id.* Thus, Intel argues that no reasonable jury could find the "request" limitations met under the doctrine of equivalents. *Id.*

There are several problems with Intel's argument. First, Intel mischaracterizes Dr. Conte's testimony by claiming that C0 residency information occurs [redacted] and [redacted] ECF No. 591 at 9. When asked whether his testimony about period signals applies to the Core_Active requests, Dr. Conte responded in the negative and further clarified that [redacted] ECF No. 603 at 10. Thus, the C0 residence information is sent "in response to" changes in the Core_Active signals sent to the PCU. Dr. Conte testified that the C0 residency counters [redacted] depending on changes in Core_Active signals, which reflect changes in core performance. ECF No. 603 at 10. Therefore, Dr. Conte's testimony cannot be understood to vitiate the "request" limitation by proving that C0 residency information is completely untethered to core performance, as Intel suggests.

Second, Intel's argument that VLSI's equivalents theory is inconsistent with the claims misconstrues Dr. Conte's testimony. Dr. Conte did not testify that the claims require the PCU to send and receive the claimed "request." *Id.* Instead, he testified that a separated core in conjunction with the PCU's internal P-Code can generate the request received by the [redacted]. 2/23 Sealed Trial Tr. 55:1-19, 57:11-15. Intel understands this as suggesting that the PCU both provides and receives the request, but VLSI's demonstrative graphically depicts the core and PCU as separate entities. *Id.* Dr. Conte distinguished the core and PCU when he testified that "the core and Core 1's P-Code" and [redacted] provided and received the request, respectively. *Id.* Moreover, to the extent Intel contends the "first master device" and "programmable clock controller" must always comprise entirely separate and distinct circuits, Intel appears to be asking this Court for a new claim construction. Even if this Court accepts Intel's characterization of the claims, Intel cannot prevail because it ultimately proposes a new claim construction, which it waived by omission. By neglecting to raise the issue to this Court in its Rule 50(a) motion, Intel has waived its right to bring a Rule 50(b) motion on this ground. And the Federal Circuit has held that the "doctrine of equivalents does not require a one-to-one correspondence between the accused device and that disclosed in the patent." *Intel Corp. v. ITC*, 946 F.2d 821, 832 (Fed. Cir. 1991); *see also Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 149 F.3d 1309, 1320 (Fed. Cir. 1998) ("[o]ne-to-one correspondence of components is not required, elements or steps may be combined without ipso facto loss of equivalency.").

This Court agrees with VLSI that substantial evidence supported the jury's finding that the Speed Shift feature satisfied the "request" limitation under the doctrine of equivalents. Intel claims JMOL of no infringement is proper for two reasons, namely that expert testimony vitiated the "request" limitation, and that the expert proposed an equivalents theory inconsistent with the claim.

But as explained above, Intel's arguments fail on both points. VLSI's presentation of Dr. Conte's testimony was sufficient to support a finding that the output of the core in combination with the code in the PCU provides the claimed "request."

2. Substantial Evidence Supports the Jury's Infringement Finding for the "Provide . . . As An Output to Control" Limitations.

Claims 14 and 17 require "provid[ing] the clock frequency of the high-speed clock as an output to control" both "a clock frequency of a second master device" and a "clock frequency of the bus," and claims 18 and 24 require "the clock controller configured to output a clock frequency of a high-speed clock to control the variable clock frequency of the bus and to control a clock frequency of a second master device coupled to the bus." '759 Patent at 8:63–64, 9:15–18, 9:26–30, 10:21–24.

The Court looks first to VLSI's doctrine of equivalents theory and the evidence it used to support its infringement claim. Dr. Conte testified that Intel's products include a PCU and clock circuit that has instructions to "provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device" 2/23 Sealed Trial Tr. 44:9-46:25, 47:17-50:17. That constitutes the programmable clock controller. *Id.* Dr. Conte also testified that the programmable clock controller includes instructions to "provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus." *Id.* at 50:18-52:20. VLSI contends this is substantial evidence to support its theory that Intel's products meet the "provide . . . as an output to control" limitations. ECF No. 603 at 13.

Intel alleges that what VLSI identified as the "second master device" in the accused products is [redacted] ECF No. 591 at 12. Because [redacted] control the clock frequency of the cores and the clock frequency of the bus, Intel argues that

VLSI's infringement theory is contrary to the plain meaning of the claims, which stipulates that the same clock frequency must be "output to control" both the second master device and the bus. *Id.* at 13. According to Intel, [redacted] is not output to either the second master device or the bus—it is output to the [redacted] respectively—and t[redacted] control the second master device and the bus. *Id.* Therefore, Intel concludes that no reasonable jury could find that the separate and independent control structure of Intel's products meets these claim limitations. *Id.*

VLSI responds that Intel's non-infringement theories ignore the claim language and the law. ECF No. 603 at 14. First, the claims do not require controlled clocks to have the same frequency and allow for different frequencies. *Id.* Second, Intel says "the same clock frequency must be 'output to control' both the second master device and the bus." ECF No. 591 at 13. Dr. Conte confirmed that the accused products meet this limitation when he explained that the same [redacted] is provided "as an output to control" both the "clock frequency of a second master device" and the "variable clock frequency of the bus." ECF No. 603 at 14. Third, the claims do not prohibit the use of intermediate components in effectuating that control, rendering Intel's non-infringement arguments based on the "[redacted] contrary to law. *Id.* at 15. The claims use the transitional term "comprising," which "is inclusive or open-ended and does not exclude additional, unrecited elements." *CollegeNet*, 418 F.3d at 1235. As Dr. Conte confirmed, "a system comprising" in the claims means that "as long as all of the elements in the claim are present, the fact that one is adding additional features or elements would not change the question of whether a product infringes." ECF No. 603 at 15.

This Court agrees that VLSI presented substantial evidence supporting the jury's infringement finding for the "provide . . . as an output to control" limitation. Intel argues that

different clock frequencies separately output by the [redacted] and [redacted] to a second master device and the bus do not satisfy the claim's plain meaning, yet in doing so Intel draws a distinction without a difference.

As VLSI points out, Intel's accused products include a PCU and clock circuit with instructions to "provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device" and "the variable clock frequency of the bus." ECF No. 603 at 13. Two critical distinctions between the accused products and the claim language, according to Intel, are that the accused products leverage intermediate hardware—that is, the [redacted] and [redacted]L instead of a PCU and clock circuit directly—to provide an output signal, and that the signals are transmitted at different frequencies. ECF No. 591 at 12. But the claims do not require that the high-speed clock transmit its output directly to the second master device or the bus. ECF No. 603 at 14. Instead, they recite a high-speed clock that produces an output *to control* the second master device or bus. *Id.* The claim's plain language does not limit "control" to direct control as Intel argues and, therefore, covers the [redacted] and [redacted] as a means for effectuating that control, especially when considering the claim's open-ended transitional term, "comprising." Further, the claims do not require the controlled clocks to have the same frequency, and if they did, expert testimony confirms that [redacted] of the same frequency to both the "clock frequency of a second master device" and the "variable clock frequency of the bus." *Id.* at 13.

Ultimately, Intel fails to meet its burden for JMOL. Even if this Court accepts Intel's arguments, they fail to prove that reasonable minds could *only* conclude that judgment of no infringement is proper. At best, Intel presents a legitimate factual dispute and critiques the logical inferences underlying the jury's conclusion. Yet JMOL is only proper when the evidence presented shows the jury would not have been at liberty to disbelieve and pointing out legitimate factual

disputes over which reasonable minds could differ fails to meet this bar. The jury relied on more than a scintilla of evidence when it weighed both parties' expert opinions, including the factual disputes embedded therein, and rendered its verdict. Therefore, this Court declines to grant JMOL of no infringement on this ground.

C. Intel's Motion for JMOL on Claims Not Argued at Trial Is Improper.

VLSI represented that it was no longer asserting indirect infringement and claimed that it reserved the right to assert those claims later. ECF No. 591 at 13. But VLSI did not dismiss its inducement or contributory infringement claims, and Intel's declaratory judgment counterclaims on both issues are still live. *Id.* Thus, Intel argues that this Court should enter judgment of no induced and no contributory infringement because VLSI did not offer any evidence at trial on either issue. *Id.* However, Federal Rule of Civil Procedure 50 states that relief in this context is appropriate only "if a party has been fully heard on an issue during a jury trial." *Rembrandt Wireless Techs., LP v. Samsung Elecs.*, 2016 WL 633909, at *5 (E.D. Tex. Feb. 17, 2016). ECF No. 603 at 15. Here, the jury could not have fully heard contributory or indirect infringement issues because, by Intel's own admission, VLSI did not assert evidence supporting either claim at trial. Accordingly, this Court denies Intel's motion on this ground as improper.

II. Substantial Evidence Supports the Jury's Verdict on Invalidity for the '759 Patent.

A patent is invalid if before the patented invention, "the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it." 35 U.S.C. § 102(g) (pre-AIA). At trial, Intel asserted that claims 14, 17, 18, and 24 of the '759 patent were invalid. The jury found that Intel did not prove by clear and convincing evidence that those claims of the '759 patent were invalid. ECF No. 564. Intel argues, however, that this Court should enter JMOL of invalidity because a reasonable jury "could only conclude" that the Yonah processor anticipates

each asserted claim. ECF No. 591 at 14. According to Intel, VLSI based its contrary assertions solely on its argument that Yonah did not have a hardware-based "programmable clock controller," but the claim language and specification foreclose VLSI's argument. *Id.*

VLSI argues there was substantial evidence for a reasonable jury to conclude that Yonah did not anticipate the '759 Patent. VLSI alleges that Intel provided bare assertions that Yonah purportedly had a "programmable clock controller" while failing to identify what in Yonah met these limitations. ECF No. 603 at 16. VLSI claims that Intel's witnesses failed to explain how any alleged "programmable clock controller" in Yonah meets the limitations of "having an embedded computer program therein" or being "coupled to the arbiter and coupled to the first master device." *Id.* at 17. VLSI further contends that Dr. Conte provided the jury with even more reason to reject Intel's flawed theory in rebuttal. *Id.* According to Dr. Conte, "Yonah is the old approach" to speed changes, whereas the '759 patent and Intel's infringing processors use "the new approach." *Id.* In the '759 patent's new approach, speed changes are controlled by a "computer-in-a-computer," *i.e.*, a "programmable clock controller with an embedded computer program." *Id.* By contrast, the operating system in Yonah made speed control decisions. *Id.* Yonah did not include a "PCU," nor any other "programmable clock controller" with "an embedded computer program" as required by the '759 patent claims. *Id.*

After losing at trial, Intel argued that "the claim language and specification make clear that a hardware-based controller is not required and that software may be used." *Id.* at 18. VLSI argues that Intel ultimately seeks a new claim construction, but Intel waived that right by failing to request a one before trial. *Id.* Notwithstanding Intel's waiver, VLSI alleges that Intel's new argument contradicts the plain claim language. *Id.* Claim 14 recites a system with hardware components, such as the programmable clock controller with an embedded computer program therein. *See* PTX-

5 ("A *system comprising*: a *bus* …; a *first master device coupled to* the bus …; and a *programmable clock controller* having an *embedded* computer program *therein*...."). Claim 18 similarly recites a system with hardware components that are "coupled to" each other. *See* PTX-5 ("A *system comprising*: a *bus* …; a *first master device coupled to* the bus; an *arbiter coupled to* the bus and *coupled to* the first master device …; and a *clock controller coupled to* the arbiter and *coupled to* the first master device …."). Contrary to Intel's assertion, the claims thus do include requirements for a hardware-based programmable clock controller. Even if Intel had presented its new theory, VLSI suggests that a reasonable jury could reach different conclusions as to whether the "operating system [being] executed in the cores of Yonah" is a "programmable clock controller having an embedded computer program therein," making JMOL improper. ECF No. 603 at 19.

This Court agrees that substantial evidence supported the jury's invalidity verdict for two reasons. First, Intel could not affirmatively show that Yonah anticipated each claim of the '759 patent, much less by clear and convincing evidence. Second, VLSI sufficiently distinguished the '759 patent from Yonah using expert testimony.

Although Intel contends that the operating system in Yonah's anticipates the "programmable clock controller" with "an embedded computer program" disclosed by the '759 patent claims, it failed to identify what they were referring to specifically. ECF No. 603 at 16. Further, Intel could not clearly articulate what in Yonah anticipated the '759 patent's limitations or how Yonah allegedly met those limitations. *Id.* Instead, Intel resorts to criticizing VLSI's distinctions between Yonah and the '759 patent. But a party cannot meet an affirmative burden of proof—here, clear and convincing evidence—by pointing to deficiencies in the opposing party's validity arguments. Indeed, Intel's generic allegations dismissing VLSI's expert testimony as "conclusory" are themselves conclusory and insufficient to meet their affirmative burden of proof.

By contrast, VLSI presented substantial evidence supporting the jury's verdict in two ways. First, VLSI pointed out deficiencies in Intel witness testimony, including the absence of any reasonable statement connecting Yonah's "programmable clock controller" and the limitations of "having an embedded computer program therein" or being "coupled to the arbiter and coupled to the first master device." ECF No. 603 at 16. Second, VLSI's distinction between Yonah as the old approach and the '759 patent as the new approach carries more weight than Intel acknowledges. Contrary to Intel's portrayal, Dr. Conte reasonably substantiated his testimony by pointing to specific differences between the two approaches—namely, the '759 patent's programmable clock controller with an "embedded computer program" as the mechanism for triggering speed changes, rather than Yonah's operating system. *Id.* at 17. Intel believes it made clear to the jury that Yonah disclosed a combination of hardware and software running on a chip, not the operating system, but that provides even more reason to preserve the jury's finding. Under Intel's theory, the jury would have clearly understood Intel's arguments when deciding against them, which increases the likelihood that they made an informed decision rather than a clearly unreasonable one warranting reversal.

"Courts grant JMOL for the party bearing the burden of proof only in extreme cases, when the party bearing the burden of proof has established its case by evidence that the jury would not be at liberty to disbelieve and the only reasonable conclusion is in its favor." *Mentor H/S, Inc. v. Medical Device Alliance, Inc.*, 244 F.3d 1365, 1375 (Fed. Cir. 2001). Here, both parties' experts provided plausible invalidity theories to the jury, which the jury was free to believe or discredit as it saw fit. Given the technical distinctions Dr. Conte drew between the '759 and the Yonah processor, this Court believes that the evidence did not weigh so heavily in Intel's favor that the jury "could have only" rendered the '759 patent invalid as Intel suggests. VLSI provided more

than a mere scintilla of legally sufficient evidence to give the jury the liberty to disbelieve either party and, therefore, adequately supported the jury's invalidity verdict.

III. Substantial Evidence Supported the Jury's Damages Award.

The jury awarded a lump sum of $1.5 billion for infringement of the '373 Patent and a lump sum of $675 million for infringement of the '759 Patent. ECF No. 564. Intel argues that it is entitled to JMOL of no damages. ECF No. 591 at 17. First, Intel alleges that no reasonable jury could value the asserted patents at $2.175 billion considering the asserted patents' sales price, the lack of a formal valuation of the asserted patents, and comparable agreements for lower amounts. *Id.* Second, Intel asserts that the jury's damages award is not supported by legally sufficient evidence because it is based on noncomparable settlement agreements. *Id.*at 17–18. Under Federal Circuit precedent, those noncomparable agreements cannot support the jury's damages award. See *Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1332, 1340 (Fed. Cir. 2009) (reversing denial of JMOL in part because damages expert relied on noncomparable licenses). Third, Intel argues that the jury's award is not supported by Dr. Sullivan's opinions. *Id.* at 18–19. Accordingly, Intel requests that this Court enter JMOL of no damages. *Id.*

VLSI responds that it presented substantial evidence supporting the damages award. First, VLSI argues Intel's patent valuation arguments rely on evidence favorable to the moving party that the jury is not required to believe. ECF No. 603 at 19. Second, VLSI alleges that there is no support for Intel's speculation that the jury based its damages numbers on noncomparable agreements. *Id.* at 20. According to VLSI, Intel "does not really know" if the jury based its award on any agreement, and a source matching an awarded number does not somehow "put the number . . . off limits to the jury." *Spectralytics, Inc. v. Cordis Corp.*, 649 F.3d 1336, 1346-47 (Fed. Cir. 2011). *Id.* Third, VLSI claims that Intel rehashes arguments previously rejected by this Court in

Daubert motions in questioning the Dr. Sullivan's reliability. *Id.* Consequently, VLSI requests that this Court deny Intel's motion for JMOL of no damages. *Id.*

This Court agrees with VLSI that the jury's damages award was supported by sufficient evidence. First, Intel alleges that the jury's $2.175 billion dollar verdict contravenes "overwhelming evidence" that the asserted patents are lower in value. But the jury considered evidence presented by both parties. This included Intel's "overwhelming evidence" of lower patent family prices, no prior ownership, and non-comparable agreements. VLSI also presented substantial evidence that Intel made over [redacted] from the nearly one billion products it sold with the infringing performance and power saving features of the patents. 2/24 Trial Tr. 593, 653-74; PDX7.74-76. The jury exercised reasonable discretion in crediting VLSI's damages evidence over Intel's damages evidence. Second, Intel contends that the jury improperly based its verdict on a non-comparable Nvidia agreement, and that Dr. Sullivan admitted as much. *Id.* Intel refuted its own argument, however, when it admitted that it "does not really know" whether the jury based its figure on any agreement. ECF No. 603 at 20. Any argument that the verdict was based on a purportedly non-comparable agreement is entirely speculative. Third, Intel argues that VLSI's damages case was unreliable, in part, because VLSI rooted it in unreliable and speculative expert testimony. ECF No. 615 at 10. But this Court has already considered and rejected these arguments in Intel's prior *Daubert* motions and its Rule 59 Motion. By asking this Court to render JMOL with no additional compelling reasons, Intel seeks to deploy the same reliability arguments and obtain different results. And contrary to Intel's argument that the damages numbers were not put into the record, Dr. Sullivan explained Intel's revenues to the jury, and any omissions were because he refrained from disclosing Intel's confidential information. 2/24 Trial Tr. 651:23–658:2; PTX3903, PTX3904.

Ultimately, Intel questions the degree to which the evidence justified the jury's verdict, but that is not the relevant question. Rather than consider how well the totality of the evidence supported the jury's finding, this Court must limit itself to determining whether the jury based its verdict on legally sufficient evidence that amounts to more than a scintilla. Here, the jury satisfied that standard by relying on the damages expert's testimony that Intel made over [redacted] dollars by infringing VLSI's patents. Intel disagrees with the outcome but falls short of proving that a verdict of no damages is the only reasonable conclusion from the evidence. Therefore, the jury's finding stands.

IV. CONCLUSION

For the reasons above, the Court finds that VLSI produced sufficient evidence to support the jury's verdict in this case. The Court therefore **DENIES** Intel's Motion for Judgment as a Matter of Law (ECF No. 591).

SIGNED this 18th day of March, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC,	§	
Plaintiff,	§	
	§	**6:21-CV-057-ADA**
v.	§	
	§	
INTEL CORPORATION,	§	
Defendant.	§	

FINAL JUDGMENT

On April 11, 2019, Plaintiff VLSI Technology LLC ("VLSI") sued Defendant Intel Corporation ("Intel") for patent infringement, including infringement of U.S. Patent Nos. 7,523,373 (the "'373 Patent"); 7,725,759 (the "'759 Patent"); and 8,156,357 (the "'357 Patent"). *See* Original Compl., ECF No. 1. Intel filed counterclaims for declaratory judgment of noninfringement and invalidity for all three patents. *See* Answer, ECF No. 171. A trial commenced on February 22, 2021, and the jury rendered a verdict on March 2, 2021. *See* Verdict, ECF No. 564. The Court has resolved all pending issues between the parties.

Therefore, pursuant to Fed. R. Civ. P. 54 and 58, the Court **ORDERS AND ENTERS FINAL JUDGMENT** as follows:

- Defendant Intel is found to have infringed claims 1, 5, 6, 9, and 11 of the '373 Patent;
- Judgment is entered against defendant Intel on its counterclaim of noninfringement of the asserted claims of the '373 Patent;
- Judgment is entered against defendant Intel on its counterclaim of invalidity of the asserted claims of the '373 Patent;

- Defendant Intel is found to have infringed claims 14, 17, 18, and 24 of the ’759 Patent;
- Judgment is entered against defendant Intel on its counterclaim of noninfringement of the asserted claims of the ’759 Patent;
- Claims 14, 17, 18, and 24 of the ’759 Patent are not invalid;
- Judgment is entered against defendant Intel on its counterclaim of invalidity of the asserted claims of the ’759 Patent;
- Defendant Intel is found not to have infringed claims 1, 11, 14, 16, or 18 of the ’357 Patent;
- Intel’s infringement of claims 1, 5, 6, 9, and 11 of the ’373 Patent and claims 14, 17, 18, and 24 of the ’759 Patent was not willful;
- The Court awards $1,500,000,000 to VLSI for Intel’s infringement of claims 1, 5, 6, 9, or 11 of the ’373 Patent;
- The Court awards $675,000,000 to VLSI for Intel’s infringement of claims 14, 17, 18, or 24 of the ’759 Patent;
- Pursuant to 35 U.S.C. § 284, the Court awards VLSI prejudgment interest in the amount of $162,321,343.
- Pursuant to 28 U.S.C. § 1961, the Court awards VLSI postjudgment interest applicable to all sums awarded, at the statutory Treasury bill rate, compounded annually, from the date of entry of this judgment until the date of payment by Intel.

SIGNED this 21st day of April, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

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(12) **United States Patent**
Russell et al.

(10) **Patent No.: US 7,523,373 B2**
(45) **Date of Patent: Apr. 21, 2009**

(54) **MINIMUM MEMORY OPERATING VOLTAGE TECHNIQUE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 294 days.

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(51) **Int. Cl.**
G01R 31/30 (2006.01)

(52) **U.S. Cl.** **714/745**; 713/300; 324/765

(58) **Field of Classification Search** 714/745, 714/721

See application file for complete search history.

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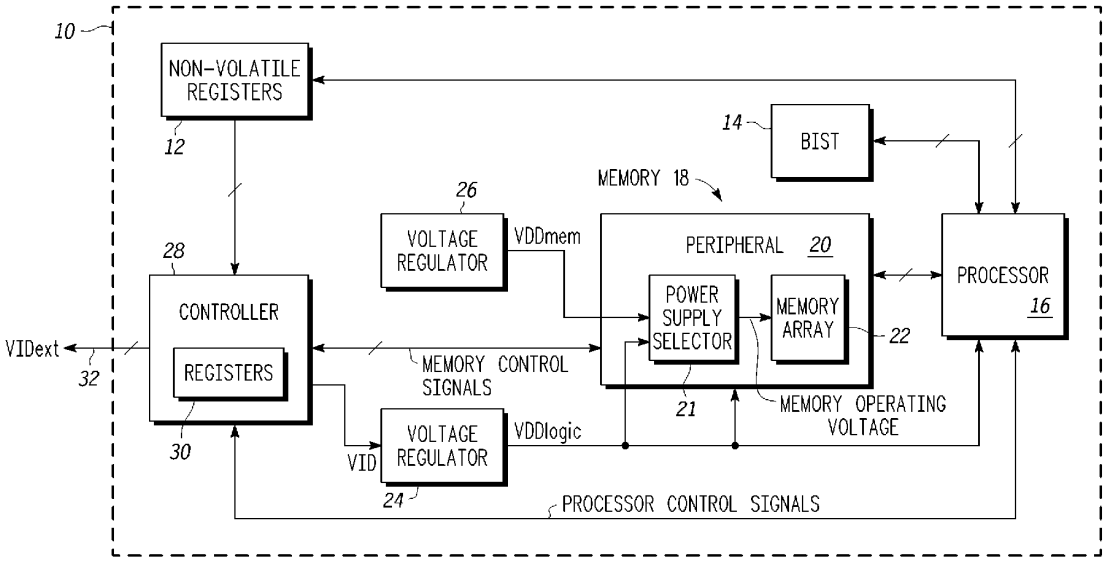
(57) **ABSTRACT**

A method includes an integrated circuit with a memory. The memory operates with an operating voltage. A value of a minimum operating voltage of the memory is determined. The value of the minimum operating voltage is stored in a non-volatile memory location that maybe a non-volatile register. This minimum operating voltage information can then be used in determining when an alternative power supply voltage may be switched to the memory or ensuring that the minimum voltage is otherwise met. The minimum voltage can be used only internal to the integrated circuit or also provided externally to a user.

16 Claims, 3 Drawing Sheets



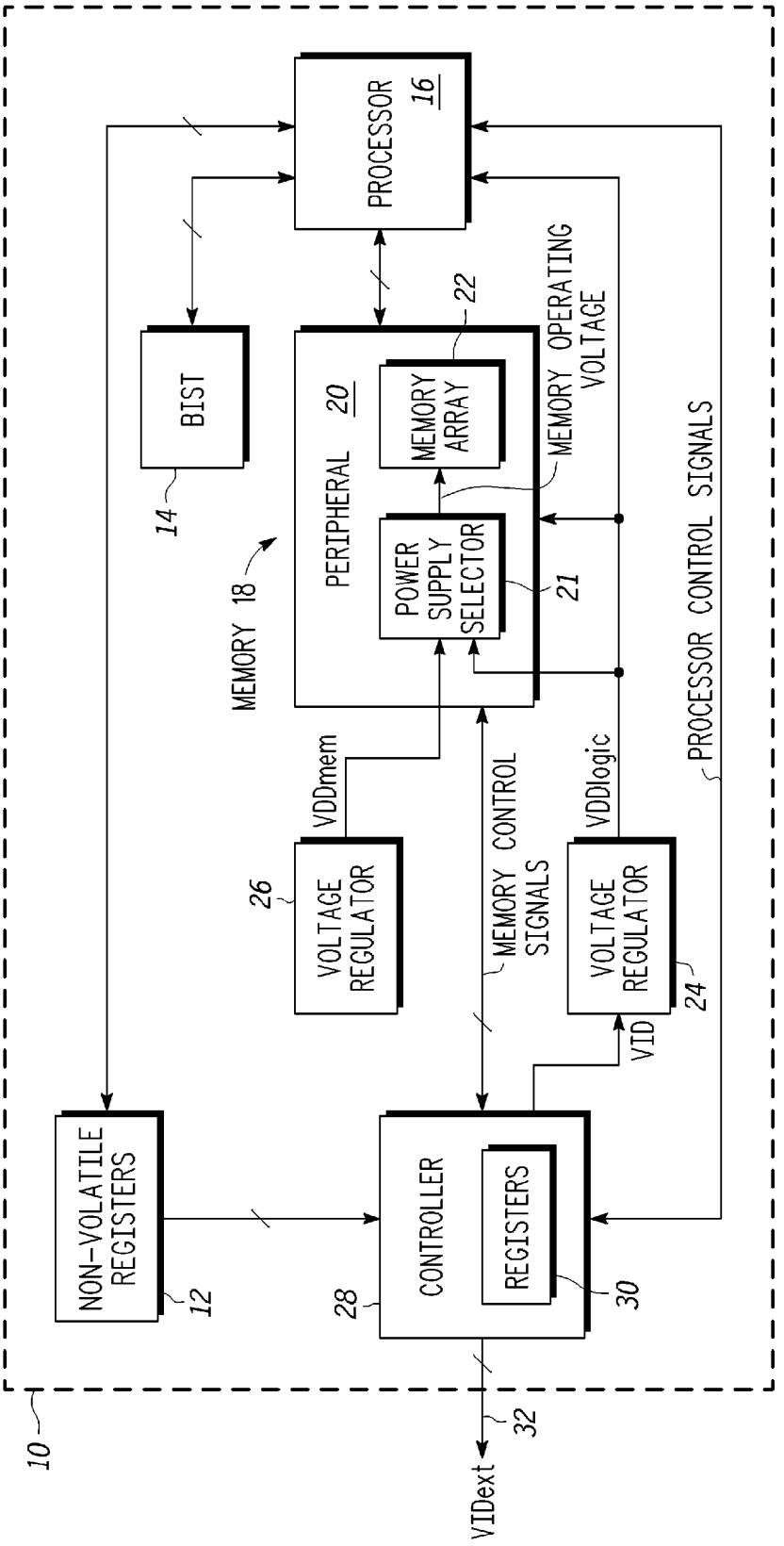

PROCESSOR 16
BIST
14
MEMORY 18
PERIPHERAL 20
MEMORY ARRAY
22
POWER SUPPLY SELECTOR
21
MEMORY OPERATING VOLTAGE
PROCESSOR CONTROL SIGNALS
VDDmem
VDDlogic
VOLTAGE REGULATOR
26
VOLTAGE REGULATOR
24
MEMORY CONTROL SIGNALS
VID
NON-VOLATILE REGISTERS
12
CONTROLLER
28
REGISTERS
30
32
VIDext
10

FIG. 1

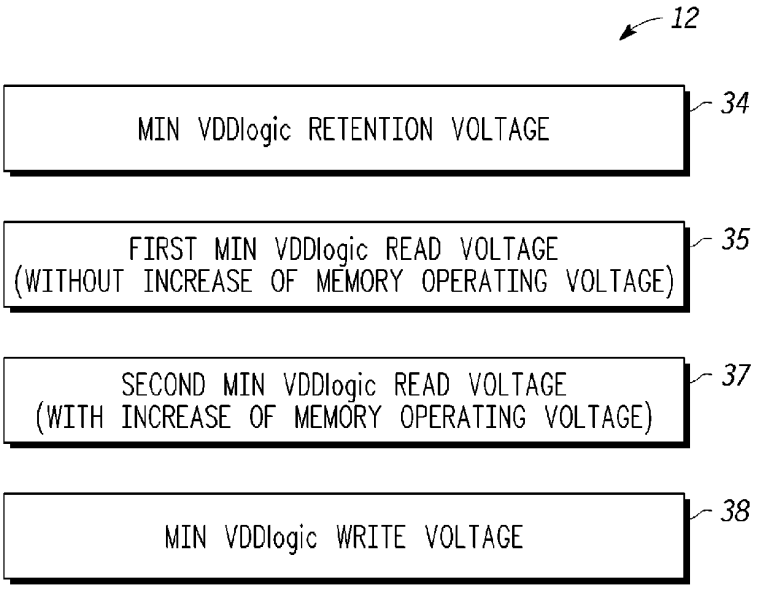

12
MIN VDDlogic RETENTION VOLTAGE
34
FIRST MIN VDDlogic READ VOLTAGE
(WITHOUT INCREASE OF MEMORY OPERATING VOLTAGE)
35
SECOND MIN VDDlogic READ VOLTAGE
(WITH INCREASE OF MEMORY OPERATING VOLTAGE)
37
MIN VDDlogic WRITE VOLTAGE
38

FIG. 2

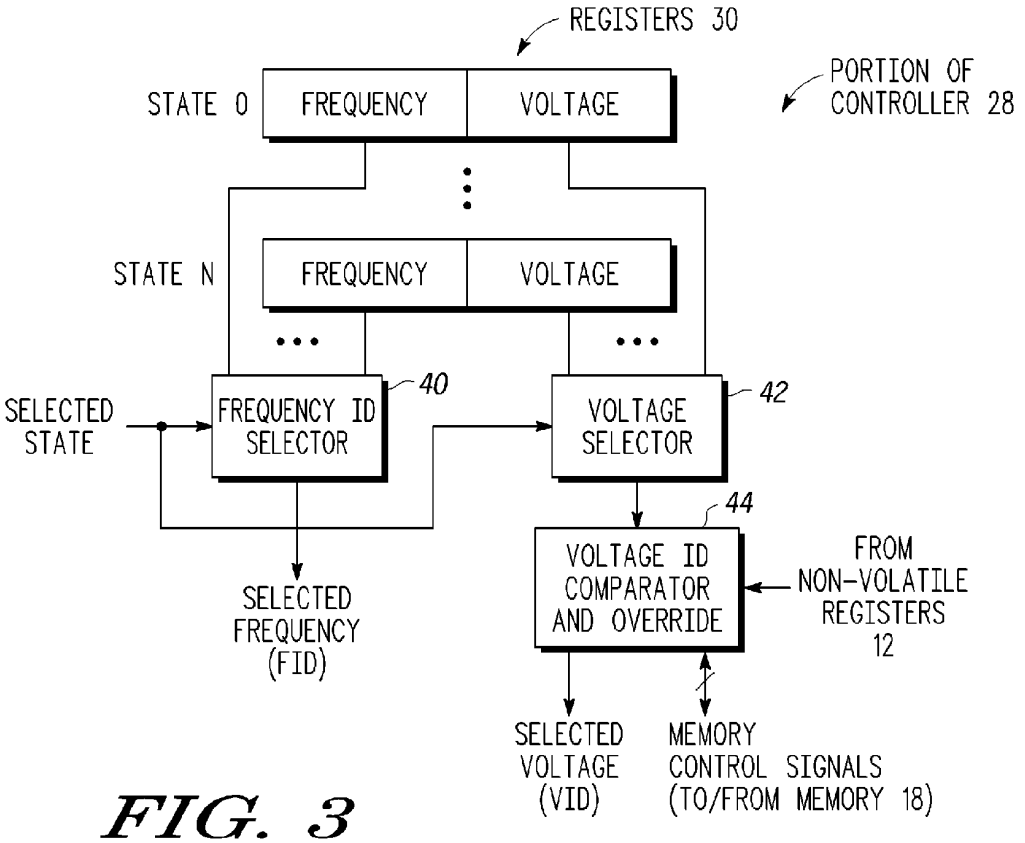

REGISTERS 30
PORTION OF CONTROLLER 28
STATE 0
FREQUENCY
VOLTAGE
STATE N
FREQUENCY
VOLTAGE
SELECTED STATE
FREQUENCY ID SELECTOR
40
VOLTAGE SELECTOR
42
44
VOLTAGE ID COMPARATOR AND OVERRIDE
FROM NON-VOLATILE REGISTERS 12
SELECTED FREQUENCY (FID)
SELECTED VOLTAGE (VID)
MEMORY CONTROL SIGNALS (TO/FROM MEMORY 18)

FIG. 3

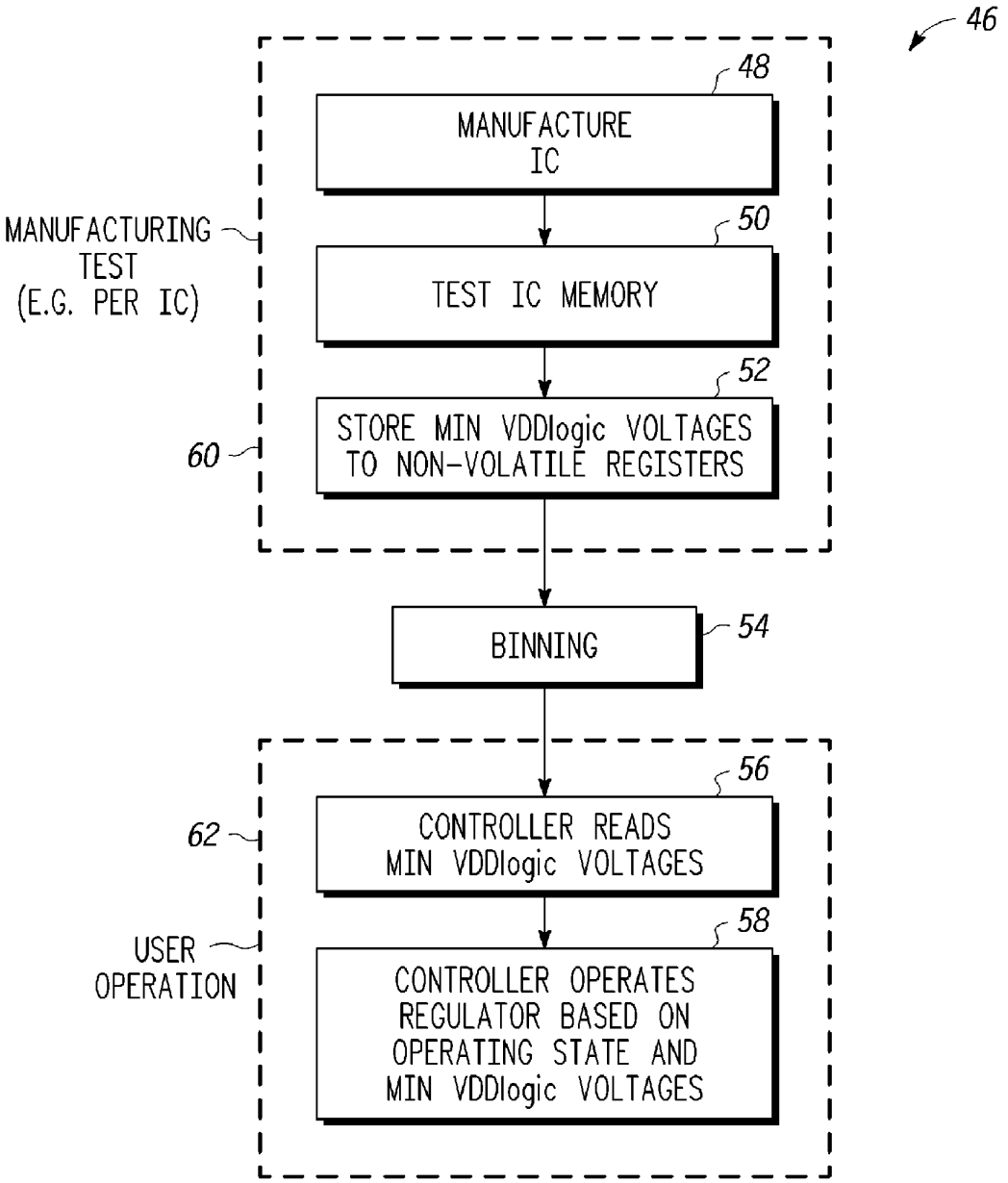

46
48
MANUFACTURE IC
MANUFACTURING TEST (E.G. PER IC)
50
TEST IC MEMORY
52
STORE MIN VDDlogic VOLTAGES TO NON-VOLATILE REGISTERS
60
BINNING
54
56
62
CONTROLLER READS MIN VDDlogic VOLTAGES
58
USER OPERATION
CONTROLLER OPERATES REGULATOR BASED ON OPERATING STATE AND MIN VDDlogic VOLTAGES

FIG. 4

MINIMUM MEMORY OPERATING VOLTAGE TECHNIQUE

FIELD OF THE INVENTION

Embodiments herein relate generally to memories, and more specifically, to a minimum memory operating voltage technique.

RELATED ART

Today, processors are typically able to operate at different voltages and frequencies, depending on the desired performance. For example, processors may operate at maximum voltage and frequency when peak performance is required, and may operate at low voltage and frequency to reduce power consumption. Therefore, tradeoffs can be made between performance and power. Similarly, such tradeoffs between performance and power can be made for other circuitry within data processing systems such as memories. That is, memories may be able to operate at higher voltages to achieve greater speed, and may also operate at lower voltages to save power. However, note that different types of circuitry within a data processing system may have different ranges of allowable operating voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements.

FIG. **1** illustrates a data processing system in accordance with one embodiment of the present invention.

FIG. **2** illustrates the non-volatile registers of FIG. **1** in accordance with one embodiment of the present invention.

FIG. **3** illustrates a portion of controller **28** in accordance with one embodiment of the present invention.

FIG. **4** illustrates a flow for testing and operating an integrated circuit, such as, for example, the data processing system of FIG. **1**, in accordance with one embodiment of the present invention.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

As used herein, the term "bus" is used to refer to a plurality of signals or conductors which may be used to transfer one or more various types of information, such as data, addresses, control, or status. The conductors as discussed herein may be illustrated or described in reference to being a single conductor, a plurality of conductors, unidirectional conductors, or bidirectional conductors. However, different embodiments may vary the implementation of the conductors. For example, separate unidirectional conductors may be used rather than bidirectional conductors and vice versa. Also, plurality of conductors may be replaced with a single conductor that transfers multiple signals serially or in a time multiplexed manner. Likewise, single conductors carrying multiple signals may be separated out into various different conductors carrying subsets of these signals. Therefore, many options exist for transferring signals.

As discussed above, tradeoffs between power and performance can be made for processors and for memory by varying the operating voltage and frequency. However, in one embodiment, the memory in a data processing system may fail at a higher voltage than the processor. That is, the processor may be able to operate at a lower voltage than is possible for the memory. Therefore, in many embodiments, the memory has a higher minimum operating voltage than the processor. Note that, as used herein, the minimum voltage or minimum operating voltage refers to a minimum which takes into consideration factors such as, for example, temperature. That is, there may be situations where the memory may actually be able to work at a voltage lower than the minimum voltage depending on, for example, factors such as temperature.

Furthermore, this minimum operating voltage for a memory varies across parts, such that one integrated circuit (IC) may tolerate one minimum operating voltage while another IC may be able to tolerate even a lower operating voltage, depending on the worst case bitcell present in each IC. Therefore, setting a particular minimum operating voltage for a type of memory, such as for a range of parts, which takes into consideration a worst case scenario for all the parts may be unnecessarily giving up the possibility for some parts to be qualified to operate at even lower voltages if those particular parts have, for example, more robust bitcells, none of which fall into the worst case scenario. Therefore, in one embodiment, each particular part, or IC, is tested to determine values for one or more minimum operating voltages, and these values of the one or more operating voltages are then stored in non-volatile memory locations on the part, such as through the use of non-volatile registers or fuses. These programmed non-volatile memory locations may then be used, for example, to bin the parts differently, control voltage during operation of the IC, etc.

FIG. **1** illustrates a block diagram of a data processing system **10** in accordance with one embodiment of the present invention. System **10** includes a processor **16**, built-in test (BIST) circuitry **14**, a memory **18**, non-volatile registers **12**, a controller **28**, and voltage regulators **24** and **26**. Processor **16** is bidirectionally coupled to non-volatile registers **12**, BIST **14**, memory **18**, and controller **28**. Memory **18** may be any type of memory, such as, for example, a static random access memory (SRAM), a dynamic random access memory (DRAM), etc. Memory **18** may be located external to processor **16**, as illustrated, or may be located within processor **16**. Memory **18** may be, for example, a cache, an embedded memory, or a stand alone memory. Memory **18** includes a memory array **22** which includes an array of bitcells which stores information. Memory **18** also includes a power supply selector **21** which receives VDDmem and VDDlogic and provides one of these to memory array **22** as the memory operating voltage. Power supply selector **21** selects one of VDDmem and VDDlogic based on information provided by controller **28** via, for example, the memory control signals. Note that in an alternate embodiment, power supply selector **21** may be located outside memory **18**. In yet another embodiment, power supply selector **21** is not present and memory **18** is permanently coupled to VDDlogic or VDDmem. Memory **18** also includes periphery circuitry **20** which includes the circuitry used to read and write memory array **22**. For example, periphery **20** may include row and column decoders, sense amplifiers, etc. In the illustrated embodiment, periphery **20** is coupled to receive VDDlogic as its power supply. Memory **18** can be any type of memory which oper-

ates as known in the art, and therefore, will only be discussed to the extent necessary to understand various embodiments of the present invention.

Controller **28** provides memory control signals to memory **18** and processor control signals to processor **16**. Controller **28** also provides a voltage identifier (VID) to voltage regulator **24** which corresponds to a desired voltage for the output of voltage regulator **24** (e.g. VDDlogic). Controller **28** may also provide one or more external voltage identifiers (VIDext) via integrated circuit terminals **32**. In an alternate embodiment, integrated circuit terminals **32** coupled to controller **28** may not be present, where controller **28** would not provide voltage identifiers externally. Controller **28** includes registers **30** which may be used to store voltage and frequency states of processor **16**. For example, in one embodiment, controller **28** may include a dynamic voltage and frequency scaling (DVFS) controller, where registers **30** includes various DVFS states, each state indicating a particular voltage and corresponding frequency, as will be described in more detail in reference to FIG. **3** below.

Voltage regulator **26** provides a substantially fixed power supply voltage, VDDmem, to power supply selector **21** of memory **18**. Voltage regulator **24**, in response to VID, provides a power supply voltage, VDDlogic, to processor **16** and memory **18** (including both periphery **20** and power supply selector **21**), where the value of VDDlogic is scalable, as controlled by the VID output of controller **28**. In one embodiment, VDDmem is greater than VDDlogic. Alternatively, VDDmem may be greater than or equal to VDDlogic.

In one embodiment, while VDDlogic remains above a minimum operating voltage required for successful reads of memory array **22**, power supply selector **21** selects VDDlogic as the memory operating voltage provided to memory array **22**, such that the memory operating voltage is substantially equal to VDDlogic. When VDDlogic is scaled to a voltage that is below the minimum memory operating voltage required for reads, power supply selector **21** selects the higher voltage, VDDmem, during read cycles to ensure that reads can still be successfully performed. In this manner, the memory operating voltage provided to memory array **22** is increased when needed to ensure successful reads (while power supply selector **21** may continue to provide the scaled down VDDlogic to memory array **22** when reads are not occurring). However, note that in one embodiment, VDDlogic may be scaled down even lower to a voltage that, even with power supply selector **21** selecting the higher VDDmem, memory **18** would no longer perform reads properly. For example, the differential between this further scaled down VDDlogic and the higher VDDmem may be so great that switching from VDDlogic to VDDmem by power supply selector **21** would result in deleterious effects, such as bit flipping where the data stored in memory array **22** is no longer accurate.

Also, in the illustrated embodiment, when VDDlogic is scaled to a voltage that is below the minimum operating voltage required for writes, write cycles cannot successfully be performed. In an alternate embodiment, another voltage regulator, similar to voltage regulator **26**, may be used to provide a substantially fixed power supply output (e.g. VDDmem-write) that is less than VDDlogic and which can be used during write cycles to help perform the write. In this embodiment, power supply selector **21** would select the lower voltage, VDDmem-write, during write cycles, as needed. For example, in this alternate embodiment, when VDDlogic is scaled to a voltage that is below the minimum operating voltage required for writes, power supply selector selects the lower voltage, VDDmem-write, during the write cycles to ensure that writes can still be successfully performed, since a lower memory operating voltage is helpful for write cycles. In this manner, the memory operating voltage provided to memory array **22** can be decreased when needed to ensure successful writes (while power supply selector **21** may continue to provide the scaled down VDDlogic to memory array **22** when writes are not occurring). Also, VDDlogic may be scaled down even lower to a voltage that, even with power supply selector **21** selecting the lower VDDmem-write to help the write cycle, memory **18** would no longer be able to perform writes properly.

Therefore, note that different types of thresholds can be defined for memory array **22**. For example, a first minimum VDDlogic read voltage may indicate the minimum VDDlogic voltage where memory array **22** can perform reads using VDDlogic rather than VDDmem. Also, a second minimum VDDlogic read voltage, which is a lower minimum than the first VDDlogic read voltage, may indicate the minimum VDDlogic voltage where memory array **22** can perform reads, even if there is a switch to the higher VDDmem. That is, when VDDlogic falls below the second minimum VDDlogic voltage, not even a switch to VDDmem may ensure proper read operations. In an alternate embodiment, note that only a single minimum VDDlogic read voltage may be indicated, such as in the case where an increase to VDDmem is not available. Also, a minimum VDDlogic write voltage may indicate the minimum VDDlogic voltage at which memory array **22** can perform write operations. In one embodiment (in which VDDmem-write, as described above, is available) first and second minimum VDDlogic write voltages can be defined, where the first minimum VDDlogic write voltage may indicate the minimum memory operating voltage allowed for writes without a decrease of the memory operating voltage to VDDmem-write and the second minimum VDDlogic write voltage (less than the first minimum VDDlogic write voltage) may indicate the minimum memory operating voltage allowed for writes even with a decrease of the memory operating voltage to VDDmem-write. Also, note that there is a minimum data retention voltage such that if the memory operating voltage falls below this minimum data retention voltage, the data in memory array **22** may be lost. Furthermore, note that there may be a minimum standby voltage for memory array **22** which represents a minimum operating voltage allowable for memory array **22** during standby.

In alternate embodiments, other types of minimum read or write operating voltages can be defined for memory array **22**. For example, in addition to the first and second minimum VDDlogic read voltages described above, other minimum read voltages may be defined such as a third minimum VDDlogic read voltage indicating the minimum voltage where memory array **22** can perform reads using VDDlogic rather than VDDmem when error correction code (ECC) is used. In this case, this third minimum VDDlogic read voltage (without increasing the memory operating voltage to VDDmem but with the use of ECC) may be less than the first minimum VDDlogic read voltage (without increasing the memory operating voltage to VDDmem and without the use of ECC) but greater than the second minimum VDDlogic read voltage (with increasing the memory operating voltage to VDDmem and without ECC). That is, by enabling ECC, a lower minimum read voltage may be acceptable for proper reads due to the use of ECC. Also, in addition to the first, second, and third minimum VDDlogic read voltages described above, a fourth minimum VDDlogic read voltage may be defined which indicates the minimum VDDlogic read voltage where memory array **22** can perform reads, even with

a switch to VDDmem and the use of ECC. In one embodiment, this fourth minimum read voltage is less than the first, second, and third minimum VDDlogic read voltages described above.

Similarly, note that the same type of minimum voltages which take into consideration the use of ECC can be defined for the minimum write voltages described above. That is, rather than defining a single minimum VDDlogic write voltage below which writes cannot be performed (as was described in reference to FIG. **1**), an alternate embodiment may instead use the first and second minimum VDDlogic write voltages described above, and may additionally use third and fourth minimum VDDlogic write voltages where ECC is also used, as was described in reference to the read voltages above.

Therefore, note that, as used herein, a minimum read voltage of memory array **22** can refer to a single minimum VDDlogic read voltage below which reads cannot be successfully performed, or may refer to one or more different types of minimum VDDlogic read voltages, such as, for example, those described above (e.g. the first, second, third, fourth minimum VDDlogic read voltages, other minimum VDDlogic read voltages, or combinations thereof). Similarly, a minimum write voltage of memory array **22** can refer to a single minimum VDDlogic write voltage below which writes cannot be successfully performed, or may refer to one or more different types of minimum VDDlogic write voltages, such as, for example, those described above (e.g. the first, second, third, fourth minimum VDDlogic write voltages, other minimum VDDlogic write voltages, or combinations thereof). Similarly, in alternate embodiments, other minimum read and write voltages may be defined which indicate different minimums depending on various other types of conditions. Also, in alternate embodiments, minimum read voltages can be combined with minimum write voltages, such that a same minimum voltage can be used for both reads and writes. Also, note that as used herein, a minimum operating voltage of memory array **22** can refer to any one or more of the minimum read, write, retention, or standby voltages (or combinations thereof) described above.

In one embodiment, controller **28** indicates to power supply selector **21** which power supply to select, VDDmem or VDDlogic (or, if available, VDDmem-write), by monitoring the VDDlogic VID selected within controller **28** (which will be described in more detail in reference to FIG. **3**) and corresponds to the desired value for VDDlogic, and determining when the VDDlogic VID indicates a voltage that is below any of the minimum VDD logic voltages described above. Also, in one embodiment, a signal may be provided by controller **28** in response to the selected VDDlogic VID being below one or more of the minimum read or write operating voltages described above.

In the illustrated embodiment, when VDDlogic is to fall below the first minimum operating voltage, power supply selector **21** selects the higher voltage, VDDmem, to increase the memory operating voltage provided to memory array **22** during reads. However, in an alternate embodiment, VDDlogic may be boosted during reads through the use of a charge pump, where this boosted VDDlogic is provided to memory array **22** for reads. In yet another embodiment, VDDmem can be provided to memory array **22** always as the memory operating voltage, where VDDmem may also be scalable such that it may be scaled down, under the control, for example, of controller **28**, to conserve power when possible (such as when it is known that reads will not be performed for a period of time).

In alternate embodiments, note that system **10** may include any number of voltage regulators used to output various different supply voltages for use by different circuitry, such as, for example, by different voltage domains within system **10** or processor **16**. Alternatively, voltage regulators **24** and **26** can be implemented as a single voltage regulator with multiple outputs. Also, in the illustrated embodiment, data processing system **10** is implemented as a single IC. However, in alternate embodiments, any number of ICs may be used. For example, in one embodiment, voltage regulators **24** and **26** may be implemented with one or more separate ICs. One or more memories such as memory **18** can also be implemented with one or more separate ICs. Processor **16** may be any type of processor such as, for example, a microcontroller, microprocessor, digital signal processor, etc., and operates as known in the art. Therefore, operation of processor **16** will only be discussed to the extent necessary to describe various embodiments of the present invention. Alternatively, processor **16** may be any type of functional circuit in system **10**. In one embodiment, the functional circuit is exclusive of memory **18**.

As described above, memory **18** has one or more minimum operating voltages, as was described above in reference to, for example, the first and second minimum VDDlogic read voltages, the minimum VDDlogic write voltage, and the minimum data retention voltage. Due to variations in manufacturing, though, these minimum operating voltages of a memory may differ across a range of parts. Therefore, one memory may have different minimum operating voltages as compared to another memory on a different IC. Therefore, in one embodiment, these minimum operating voltages are determined for each part and stored in non-volatile registers on each part. For example, in one embodiment, memory **18** is tested to determine the minimum operating voltages and these voltages or values representative of these voltages are then stored in non-volatile registers **12**.

For example, referring to FIG. **1**, BIST **14** may include any type of circuitry to perform any type of built-in self test. In one embodiment, BIST **14** includes circuitry used to test for minimum operating voltages for memory **18**. For example, BIST **14** may include circuitry to determine one or more of the minimum operating voltages discussed above. BIST **14** may also include other circuitry for determining other types of minimum operating voltages or other parameters. BIST **14** may return these values to processor **16** which may then provide these values to be written to non-volatile registers **12**.

FIG. **2** illustrates one embodiment of non-volatile registers **12**. The embodiment of FIG. **2** includes one or more registers which store a minimum VDDlogic retention voltage **34** and a first minimum VDDlogic read voltage **35** (without the increase of the memory operating voltage). Note that the minimum VDDlogic read voltage **35** (without the increase of the memory operating voltage) refers to the minimum voltage VDDlogic should have (within normal margins) in order for reads to be performed successfully. Note also that as long as VDDlogic is at or above this minimum voltage, the memory operating voltage need not be increased to the higher VDDmem, as was described above. That is, so long as VDDlogic is at or above this minimum voltage, VDDlogic can be provided as the memory operating voltage.

Note that first minimum VDDlogic read voltage **35** may also be referred to as a minimum read memory operating voltage. That is, while VDDlogic remains above the first minimum VDDlogic read voltage, the memory operating voltage is substantially equal to VDDlogic. The first minimum VDDlogic read voltage **35** may also be referred to as a minimum switching voltage since these values can be used to

determine when a switch is to be performed from one regulated power supply (e.g. VDDlogic) to another regulated power supply (e.g. VDDmem).

In the illustrated embodiment of FIG. **2**, non-volatile registers **12** also store a second minimum VDDlogic read voltage **37** (with the increase of the memory operating voltage). As was described above in reference to FIG. **1**, there is a point where VDDlogic may be scaled down to such a level that even with power supply selector **21** selecting the higher VDDmem, operation of memory **18** may still fail. For example, this may be due to the large differential in voltage values between the scaled down VDDlogic and the higher VDDmem. Therefore, in one embodiment, BIST **14** may also include circuitry to determine these minimums, and processor **16** may therefore also store these minimums in non-volatile registers **12**.

In the illustrated embodiment of FIG. **2**, non-volatile registers **12** also store a minimum VDDlogic write voltage **38** which, as described above, can refer to the minimum voltage VDDlogic must have (within normal margins) in order for writes to be performed successfully. Note that minimum VDDlogic write voltage **38** may also be referred to as the minimum write memory operating voltage. In an alternate embodiment, non-volatile registers **12** can instead include a first and a second minimum VDDlogic write voltage (corresponding to minimum VDDlogic write voltages without or with a decrease to VDDmem-write, respectively). In this alternate embodiment, note that the first minimum VDDlogic write voltage can also be referred to as a minimum write memory operating voltage or a minimum switching voltage, for reasons analogous to those provided above with respect to first minimum VDDlogic read voltage **35**.

Note that in the example of FIG. **2**, separate read and write voltages are provided; however, they may be combined such that a same or single minimum is set for both reads and writes. Also, note that any number of non-volatile registers may be used. Furthermore, any number of minimum operating voltages or other operating parameters of memory **18** may be included. For example, in one embodiment, second minimum voltage **37** may not be present, or other minimum operating voltages, such as a minimum standby voltage or those that were described above in reference to the use of ECC, may be present. Also, minimums for various different memories present within a system may be stored into non-volatile registers **12**. In one embodiment, encoded versions of the minimum voltages (i.e. VIDs for each minimum voltage) may be stored instead where encoded versions of the operating voltages (e.g. VDDlogic VIDs) are monitored. In one embodiment, non-volatile registers **12** may be implemented as programmable fuses. Alternatively, they may be implemented as volatile registers. For example, in one embodiment, the volatile registers may store minimum operating voltages that represent the worst case across a group of parts.

Also, note that there may be other ways to determine these minimum values stored into non-volatile registers **12**. That is, BIST **14** may not be present, or, even if present, BIST **14** may not perform the determination of the minimum operating voltages. In an alternate embodiment, an external tester may be used to apply a testing protocol external from system **10** during or after manufacture of system **10** to determine the minimum operating voltages. That is, other testing circuitry, either internal to system **10** or external to system **10**, may be used to determine these values. In yet another alternate embodiment, different types of algorithms may be used to determine these values for each memory (i.e. for each IC or part).

In one embodiment, regardless of whether BIST **14** is used or another tester is used, the determination of the minimum operating voltages is made specifically for memory **18** (and may be made specifically for any number of memories that may be present in system **10**). That is, each memory can be separately characterized with these minimum operating voltages which may allow, for example, for improved binning, for improved customer control, etc. By making the determination specifically per memory (i.e. per part or IC), a user or customer does not need to assume and plan for a worst case scenario across all parts because they may have one or more parts that actually works better. That is, by binning according to the worst case scenario, a particular part may be restricted from use even though that particular part is capable of operating at a voltage below what binning allows. Other examples of how to make use of the information in non-volatile registers **12** will be discussed in reference to FIGS. **3** and **4**.

FIG. **3** illustrates one embodiment of a portion of controller **28**. Registers **30** includes N+1 registers, each corresponding to a voltage/frequency state. That is, a corresponding encoded frequency and voltage is provided for each of state 0 through state N (where each of state 0 through N may be referred to as a DVFS state). Controller **28** may provide a selected state signal to select a DVFS state (where controller **28** may provide this signal based on a state selected by processor **16**). The selected state signal is provided to frequency selector **40** to select one of the N+1 states, such that the selected frequency is provided by frequency selector **40**. The selected state signal is also provided to voltage selector **42** such that voltage selector **42** provides the corresponding selected encoded voltage to a comparator and override **44**. Therefore, the frequency and voltage states selected by the selected state signal correspond to the desired frequency and voltage. For example, the selected voltage state corresponds to the desired voltage value for VDDlogic. Comparator and override **44** uses the information stored in non-volatile registers **12** to determine if the selected voltage value output by voltage selector **42** (i.e. the desired voltage value for VDDlogic) is appropriate for memory **18**. For example, if the selected voltage value is below second minimum read voltage **37** or minimum write voltage **38**, operation of memory **18** may fail. In this case, comparator and override **44** may force a different voltage selection that remains above the appropriate minimum voltage. Therefore, controller **28** may adjust VID accordingly to prevent regulator **24** from outputting the desired voltage selected by the selected state signal. Therefore, while the selected frequency may remain low, the corresponding selected low voltage is overridden to help ensure continued proper operation of memory **18**.

Similarly, comparator and override **44** can use first minimum VDDlogic read voltage **35** to determine whether an increase to VDDmem is needed. That is, if the voltage selected by voltage selector **42** in response to the selected state signal indicates a voltage that is less than first minimum VDDlogic read voltage **35** (but still greater than second minimum VDDlogic read voltage **37**), comparator and override **44** can send a signal to power supply selector **21** (via the memory control signals) to indicate to power supply selector **21** to select VDDmem rather than VDDlogic to provide as the memory operating voltage to memory array **22**. In an alternate embodiment in which VDDmem-write is also used (along with first and second minimum VDDlogic write voltages), comparator and override **44** can send a signal to power supply selector **21** to indicate when a switch from VDDlogic to VDDmem-write is needed. Therefore, comparator and override **44** can adjust or override the selected voltage VID to control VDDlogic as needed, as well as signal to power supply selector **21** when a switch in power supply voltages is needed. Comparator and override **44** can make these adjust-

ments or send these signals in response to comparing the selected or desired voltage with one or more of the various minimum operating voltages that are stored in non-volatile registers **12**.

FIG. **4** illustrates a flow **46** which may be used to determine and use the minimum operating voltages of FIG. **2**. For example, flow **46** includes a manufacturing test portion **60** which is performed per part (i.e. per IC), and includes a user operation portion **62**. Manufacturing test portion **60** includes manufacturing the IC (block **48**) and testing the IC memory (block **50**). For example, as discussed above, this may be performed by BIST **14** or some other tester or method of testing. Manufacturing test portion **60** also includes storing the values of the minimum VDDlogic voltages or values representative of the actual values, determined by the IC testing performed in block **50**, to the non-volatile registers of the IC being tested, such as non-volatile registers **12**,(block **52**). In one embodiment, the minimum VDDlogic voltages can be determined per a group of parts or ICs. For example, testing can be performed on a representative IC of a particular lot, where those values are stored in the non-volatile registers of each IC in the lot.

After manufacturing test portion **60**, the stored values may be used for improved power binning. For example, the tested ICs may be binned according to finer power or speed bins since each part is tested individually for the minimum VDDlogic voltages. Furthermore, a customer can be given more precise information about each specific IC as opposed to relying on a global set of worst case minimums.

After binning **54**, flow **46** enters user operation portion **62**. User operation portion **62** includes using a controller (such as controller **28**) to read the minimum VDDlogic voltages (in block **56**) and operating a regulator (such as regulator **26**) based on an operating state (such as one of state 0 to N) and on the minimum VDDlogic voltages (in block **58**). That is, as was described in reference to FIG. **3**, controller **28** may control regulator **24** based on both the selected state of state 0 to N and the information stored in non-volatile registers **12**. For example, controller **28** may use the information stored in non-volatile registers **12** to selectively override all or a portion of the selected state.

By now it should be appreciated that there has been provided a technique for determining and storing specific minimum operating voltages for each IC. In this manner, by determining and storing this information unique to each IC (i.e. by separately characterizing each IC), an IC may be operated at its lowest voltage. For example, by binning according to the worst case scenario, an IC may be restricted from use even though a particular IC or part is capable of operating at a voltage below what binning allows. This can be addressed by determining and storing information unique to each IC, as discussed above. Also, with the stored information, the increase of the memory operating voltage (such as from VDDlogic to VDDmem, as was described above), may be performed only when needed by using the stored first minimum values as triggering points for increasing the memory operating voltage rather than relying on a global value (i.e. a value that is common to all ICs). For example, if global values are relied on rather than the particular values determined for each IC, a power selector may switch to a higher power supply voltage (such as VDDmem) when it really was not necessary because the particular IC may have been able to operate properly at the lower voltage, thus unnecessarily consuming power. Furthermore, the decision to increase the memory operating voltage can also be made without a user's knowledge or intervention.

In one embodiment, a method includes providing an integrated circuit with a memory, operating the memory with an operating voltage, determining a value of a minimum operating voltage of the memory, providing a non-volatile memory (NVM) location, and storing the value of the minimum operating voltage of the memory in the NVM location.

In a further embodiment, the step of testing the memory is further characterized by the minimum operating voltage comprising one of a group consisting of minimum retention voltage, minimum write voltage, minimum read voltage, and a minimum standby voltage.

In another further embodiment, the step of providing the integrated circuit with the memory is further characterized by the memory comprising one of a group consisting of dynamic random access memory and static random access memory.

In another further embodiment, the step of providing the NVM location is further characterized by the NVM location comprising a non-volatile register.

In another further embodiment, the method further includes providing a functional circuit on the integrated circuit exclusive of the memory, providing a first regulated voltage to the functional circuit, providing a second regulated voltage, and providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage and the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage. In yet a further embodiment, the method further includes determining a value of a minimum switching voltage of the first regulated voltage for switching from the first regulated voltage to the second regulated voltage in response to the first regulated voltage going below the minimum operating voltage, and storing the value of the minimum switching voltage in the NVM location. In yet a further embodiment, the method further includes providing a signal in response to a desired value for the first regulated voltage being below the minimum operating voltage.

In another further embodiment, the method further includes providing a controller on the integrated circuit that selects an operating value for the operating voltage of the memory, and providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage.

In another further embodiment, the method further includes providing the value of the minimum operating voltage external to the integrated circuit.

In another further embodiment, the step of determining is further characterized as performing a test applied externally from the integrated circuit.

In another embodiment, an integrated circuit includes a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage, and a memory location that stores a value representative of the minimum operating voltage.

In a further embodiment of the another embodiment, the integrated circuit further includes a first voltage regulator for supplying a first regulated voltage, a circuit that provides a function and uses the first regulated voltage, a second voltage regulator for supplying a second regulated voltage, and a power supply selector that supplies the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the minimum operating voltage and supplies the second regulated voltage as the operating voltage when the first regulated voltage is below the minimum operating voltage. In yet a further embodiment of the another

embodiment, the circuit that provides a function includes a processor, and the integrated circuit further includes a built-in self test (BIST) circuit, coupled to the processor, useful in determining the minimum operating voltage. In another yet further embodiment, the memory is further characterized as having a value of a minimum switching voltage of the first regulated voltage for switching from the first regulated voltage to the second regulated voltage in response to the first regulated voltage going below the minimum operating voltage, and the memory location is further characterized as storing the value of the minimum switching voltage.

In another further embodiment of the another embodiment, the minimum operating voltage comprises one of a group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage. In yet a further embodiment, the minimum operating voltage comprises another one of the group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage.

In another further embodiment of the another embodiment, the memory comprises one of a group consisting of a static random access memory and a dynamic random access memory.

In another further embodiment of the another embodiment, the integrated circuit includes a processor that selects an operating value for the operating voltage of the memory, and means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage.

In another further embodiment of the another embodiment, the memory location is characterized as being a non-volatile register.

In yet another embodiment, a method includes providing an integrated circuit with a memory that uses an operating voltage, testing the memory to determine the operating voltage of the memory that is a minimum operating voltage, and storing, in a non-volatile manner, the value of the minimum operating voltage.

In a further embodiment of the yet another embodiment, the method further includes providing a functional circuit on the integrated circuit exclusive of the memory, providing a first regulated voltage to the functional circuit, providing a second regulated voltage, and providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage and the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Some of the above embodiments, as applicable, may be implemented using a variety of different data processing systems. For example, although FIG. **1** and the discussion thereof describe an exemplary data processing system architecture, this exemplary architecture is presented merely to provide a useful reference in discussing various aspects of the invention. Of course, the description of the architecture has been simplified for purposes of discussion, and it is just one of may different types of appropriate architectures that may be used in accordance with the invention. Those skilled in the art will recognize that the boundaries between logic blocks are merely illustrative and that alternative embodiments may merge logic blocks or circuit elements or impose an alternate decomposition of functionality upon various logic blocks or circuit elements.

Furthermore, those skilled in the art will recognize that boundaries between the functionality of the above described operations are merely illustrative. The functionality of multiple operations may be combined into a single operation, and/or the functionality of a single operations may be distributed in additional operations. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

The term "plurality", as used herein, is defined as two or more than two. The term another, as used herein, is defined as at least a second or more.

The term "coupled", as used herein, is defined as connected, although not necessarily directly, and not necessarily mechanically.

Because the above detailed description is exemplary, when "one embodiment" is described, it is an exemplary embodiment. Accordingly, the use of the word "one" in this context is not intended to indicate that one and only one embodiment may have a described feature. Rather, many other embodiments may, and often do, have the described feature of the exemplary "one embodiment." Thus, as used above, when the invention is described in the context of one embodiment, that one embodiment is one of many possible embodiments of the invention.

Notwithstanding the above caveat regarding the use of the words "one embodiment" in the detailed description, it will be understood by those within the art that if a specific number of an introduced claim element is intended in the below claims, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such limitation is present or intended. For example, in the claims below, when a claim element is described as having "one" feature, it is intended that the element be limited to one and only one of the feature described.

Furthermore, the terms "a" or "an", as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an"

limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles.

What is claimed is:

1. A method, comprising:
providing an integrated circuit with a memory;
operating the memory with an operating voltage;
determining a value of a minimum operating voltage of the memory;
providing a non-volatile memory (NVM) location;
storing the value of the minimum operating voltage of the memory in the NVM location;
providing a functional circuit on the integrated circuit exclusive of the memory;
providing a first regulated voltage to the functional circuit;
providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;
providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and
providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

2. The method of claim **1**, wherein the step of testing the memory is further characterized by the minimum operating voltage comprising one of a group consisting of minimum write voltage, minimum read voltage, and a minimum standby voltage.

3. The method of claim **1**, wherein the step of providing the integrated circuit with the memory is further characterized by the memory comprising one of a group consisting of dynamic random access memory and static random access memory.

4. The method of claim **1**, wherein the step of providing the NVM location is further characterized by the NVM location comprising a non-volatile register.

5. The method of claim **1**, further comprising:
providing a signal in response to a desired value for the first regulated voltage being below the minimum operating voltage.

6. The method of claim **1**, further comprising:
providing a controller on the integrated circuit that selects an operating value for the operating voltage of the memory; and
providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage.

7. The method of claim **1**, further comprising providing the value of the minimum operating voltage external to the integrated circuit.

8. The method of claim **1**, wherein the step of determining is further characterized as performing a test applied externally from the integrated circuit.

9. An integrated circuit, comprising:
a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage;
a memory location that stores a value representative of the minimum operating voltage;
a first voltage regulator for supplying a first regulated voltage;
a circuit that provides a function and uses the first regulated voltage;
a second voltage regulator for supplying a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage; and
a power supply selector that supplies the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the minimum operating voltage and supplies the second regulated voltage as the operating voltage when the first regulated voltage is below the minimum operating voltage, wherein while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage.

10. The integrated circuit of claim **9**, wherein the circuit that provides a function comprises a processor, further comprising: a built-in self test (BIST) circuit, coupled to the processor, which determines the minimum operating voltage.

11. The memory of claim **9**, wherein the minimum operating voltage comprises one of a group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage.

12. The memory of claim **11**, wherein the minimum operating voltage comprises another one of the group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage.

13. The memory of claim **9**, wherein the memory comprises one of a group consisting of a static random access memory and a dynamic random access memory.

14. The memory of claim **9**, further comprising:
a processor that selects an operating value for the operating voltage of the memory; and
means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage.

15. The memory of claim **9**, wherein the memory location is characterized as being a non-volatile register.

16. A method, comprising:
providing an integrated circuit with a memory that uses an operating voltage;
testing the memory to determine the operating voltage of the memory that is a minimum operating voltage;
storing, in a non-volatile manner, the value of the minimum operating voltage;
providing a functional circuit on the integrated circuit exclusive of the memory;
providing a first regulated voltage to the functional circuit;
providing a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage;
providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and
providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

* * * * *

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(12) **United States Patent**
Henson

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(45) **Date of Patent: May 25, 2010**

(54) **SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE**

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(58) **Field of Classification Search** 713/300, 713/322, 500–503, 400–401, 600–601; 710/15, 710/309

See application file for complete search history.

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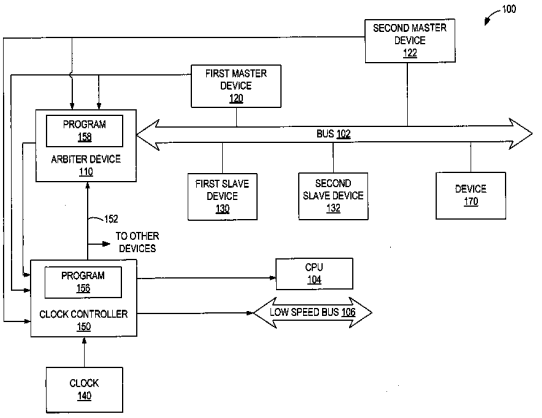
(57) **ABSTRACT**

A method of controlling a clock frequency is disclosed and includes monitoring a plurality of master devices that are coupled to a bus within a system. The method also includes receiving an input from at least one of the plurality of master devices. The input can be a request an increase to the clock frequency of the bus. Further, the method includes selectively increasing the clock frequency of the bus in response to the request.

27 Claims, 6 Drawing Sheets



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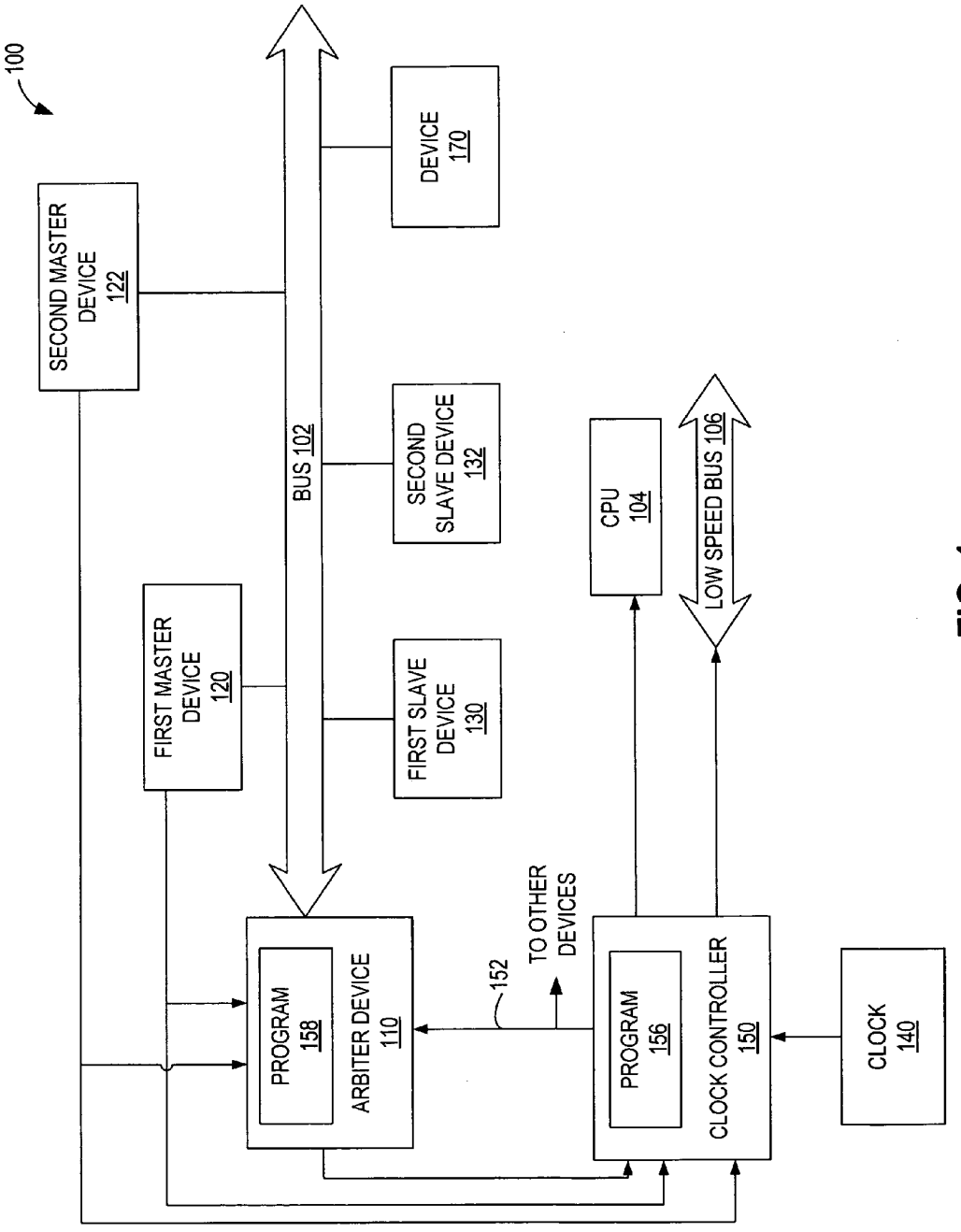
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SECOND MASTER DEVICE 122
DEVICE 170
BUS 102
SECOND SLAVE DEVICE 132
CPU 104
LOW SPEED BUS 106
FIRST MASTER DEVICE 120
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TO OTHER DEVICES
152
PROGRAM 158
ARBITER DEVICE 110
PROGRAM 156
CLOCK CONTROLLER 150
CLOCK 140

FIG. 1

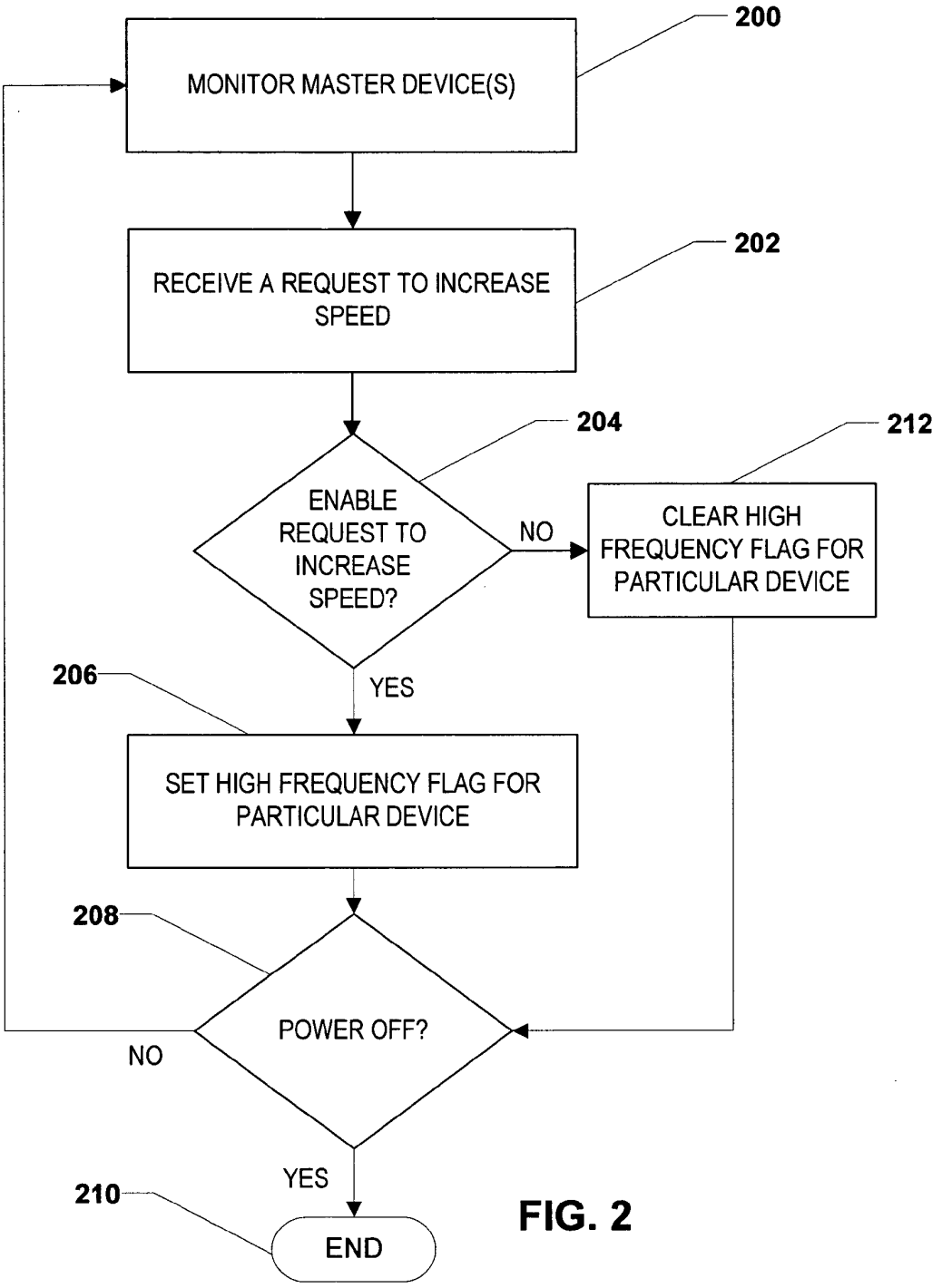
200
MONITOR MASTER DEVICE(S)
202
RECEIVE A REQUEST TO INCREASE SPEED
204
ENABLE REQUEST TO INCREASE SPEED?
NO
212
CLEAR HIGH FREQUENCY FLAG FOR PARTICULAR DEVICE
YES
206
SET HIGH FREQUENCY FLAG FOR PARTICULAR DEVICE
208
POWER OFF?
NO
YES
210
END

FIG. 2

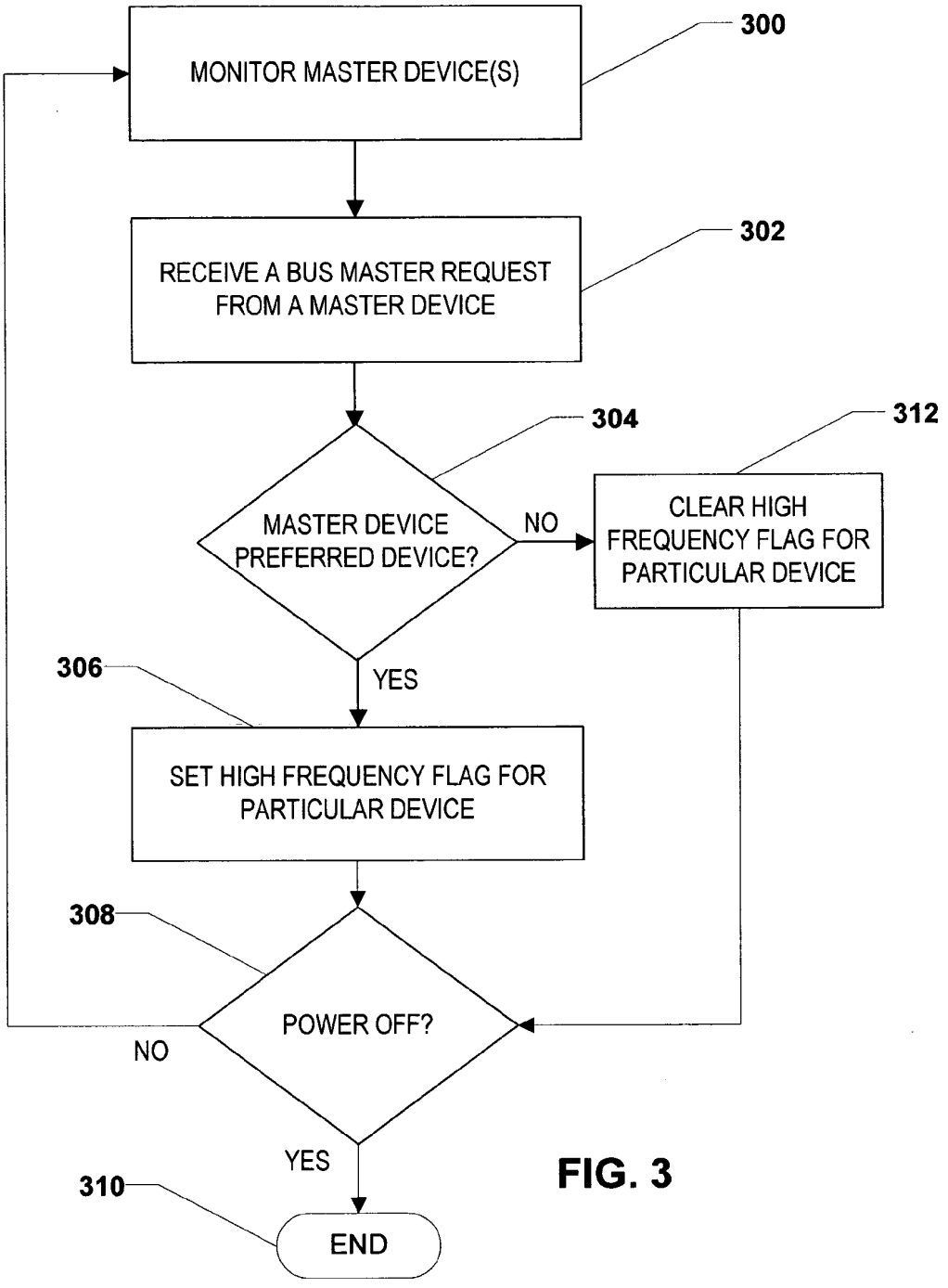
MONITOR MASTER DEVICE(S)
300
RECEIVE A BUS MASTER REQUEST FROM A MASTER DEVICE
302
MASTER DEVICE PREFERRED DEVICE?
304
NO
CLEAR HIGH FREQUENCY FLAG FOR PARTICULAR DEVICE
312
YES
306
SET HIGH FREQUENCY FLAG FOR PARTICULAR DEVICE
308
POWER OFF?
NO
YES
310
END

FIG. 3

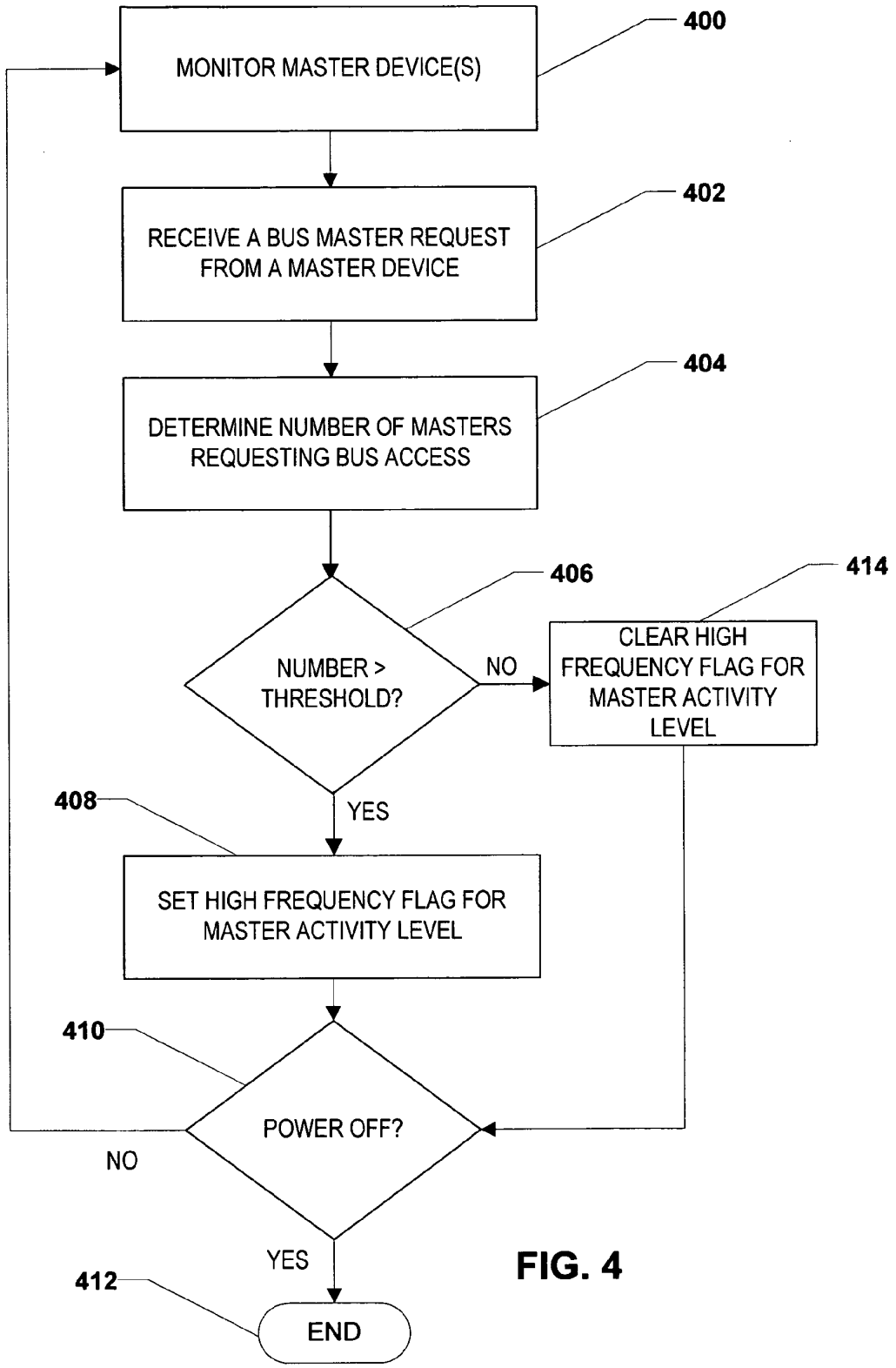
MONITOR MASTER DEVICE(S)
400
RECEIVE A BUS MASTER REQUEST FROM A MASTER DEVICE
402
DETERMINE NUMBER OF MASTERS REQUESTING BUS ACCESS
404
406
NUMBER > THRESHOLD?
NO
414
CLEAR HIGH FREQUENCY FLAG FOR MASTER ACTIVITY LEVEL
YES
408
SET HIGH FREQUENCY FLAG FOR MASTER ACTIVITY LEVEL
410
POWER OFF?
NO
YES
412
END

FIG. 4

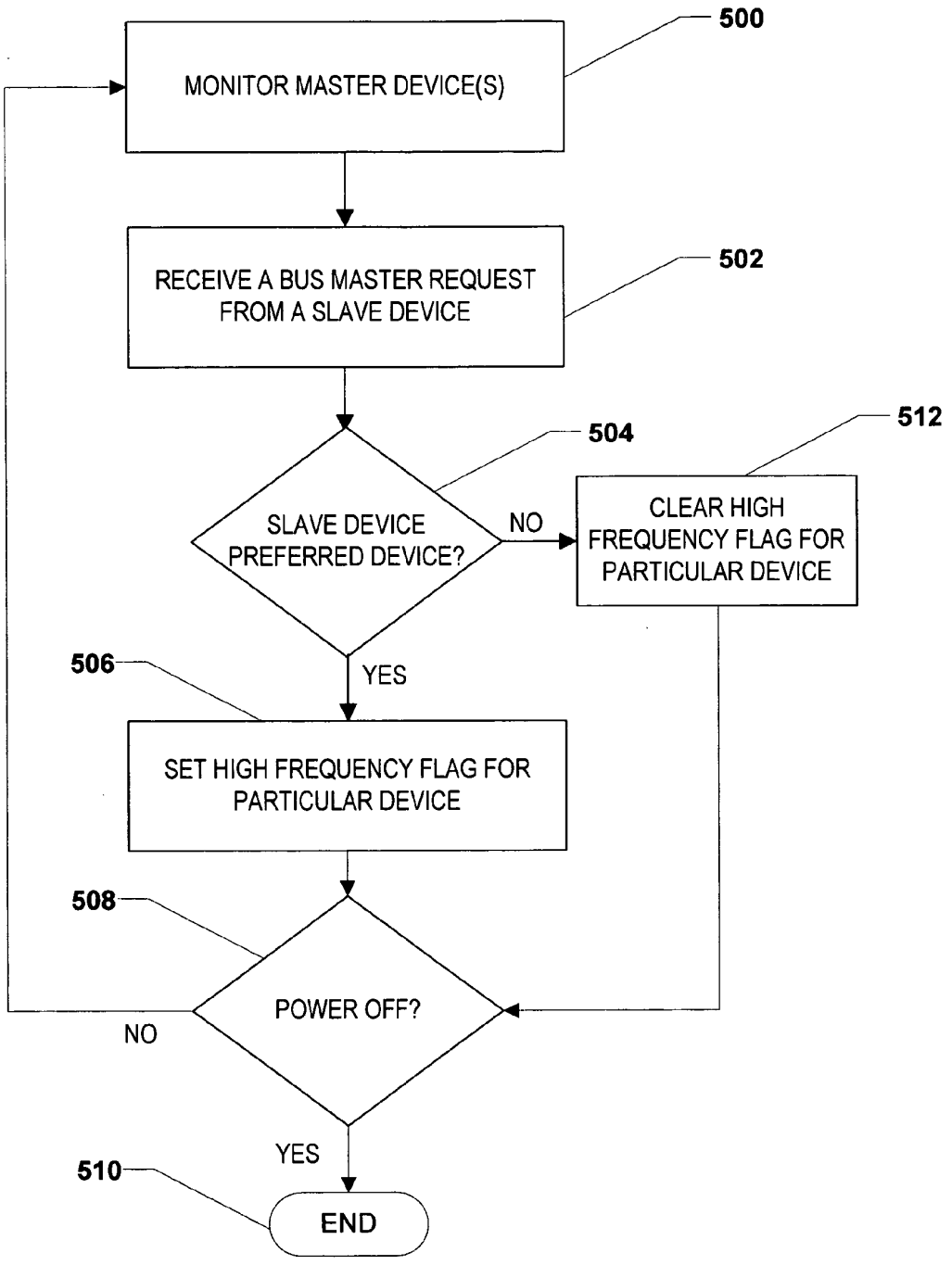
500
MONITOR MASTER DEVICE(S)
502
RECEIVE A BUS MASTER REQUEST FROM A SLAVE DEVICE
504
SLAVE DEVICE PREFERRED DEVICE?
NO
512
CLEAR HIGH FREQUENCY FLAG FOR PARTICULAR DEVICE
YES
506
SET HIGH FREQUENCY FLAG FOR PARTICULAR DEVICE
508
POWER OFF?
NO
YES
510
END

FIG. 5

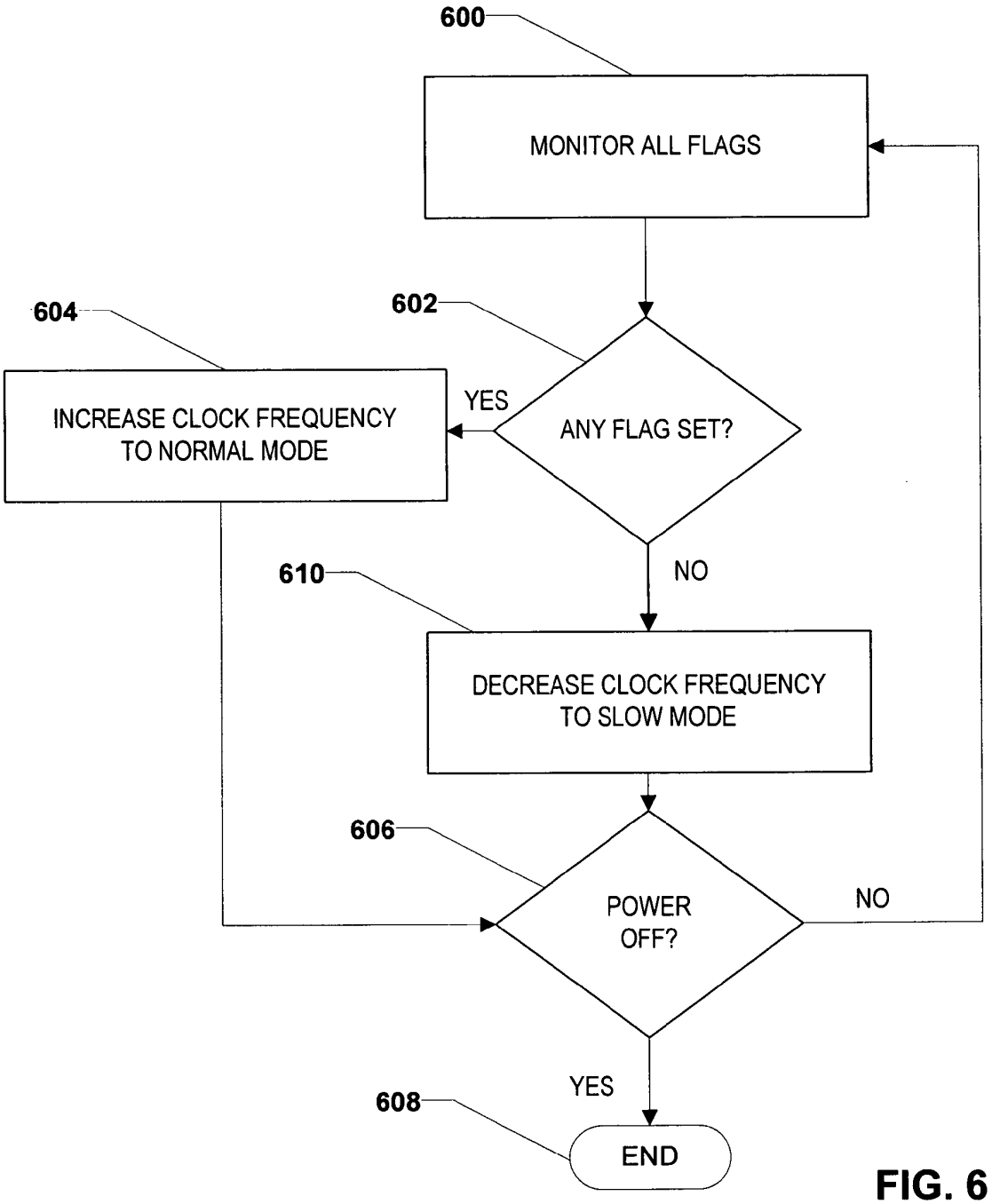
600
MONITOR ALL FLAGS
602
ANY FLAG SET?
YES
604
INCREASE CLOCK FREQUENCY TO NORMAL MODE
NO
610
DECREASE CLOCK FREQUENCY TO SLOW MODE
606
POWER OFF?
NO
YES
608
END

FIG. 6

SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE

FIELD OF THE DISCLOSURE

The present disclosure relates to electronic devices and to managing clock speeds within electronic devices.

BACKGROUND

As technology advances, portable multimedia devices are being designed with increased functionality and increased efficiency to support that functionality. For example as storage within portable audio players, such as an MPEG-1 Audio Layer-3 (MP3) player, increases, the need to quickly and efficiently access stored audio files also increases. One way to increase the performance of the MP3 player and provide quicker access to stored files is to increase the clock frequency of the clock used in the device. However, as the clock frequency increases to deliver more performance, the power consumption of the MP3 player also increases.

Accordingly, there is a need for an improved system and method of controlling a clock frequency in an electronic device in order to selectively deliver faster clock speeds.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram that illustrates an electronic system;

FIG. **2** is a flow chart illustrating a method of setting bus speed control flags within an electronic system is shown;

FIG. **3** is a flow chart illustrating an alternative embodiment of a method of setting bus speed control flags within an electronic system is shown;

FIG. **4** is a flow chart illustrating an alternative embodiment of a method of setting bus speed control flags within an electronic system is shown;

FIG. **5** is a flow chart illustrating yet another alternative embodiment of a method of setting bus speed control flags within an electronic system is shown; and

FIG. **6** is a flow chart illustrating a method of monitoring one or more speed control flags within an electronic system.

DETAILED DESCRIPTION OF DRAWINGS

A method of controlling a clock frequency is disclosed and includes monitoring a plurality of master devices that are coupled to a bus within a system. The method also includes receiving an input from at least one of the plurality of master devices. The input can be a request for an increase to the clock frequency of the bus. Further, the method includes selectively increasing the clock frequency of the bus in response to the request.

In a particular embodiment, the method includes determining whether to enable the request to increase the clock frequency of the bus and setting a high frequency flag. In another particular embodiment, the method includes clearing the high frequency flag. Additionally, in yet another particular embodiment, the method includes monitoring a plurality of high frequency flags and increasing a clock frequency when at least one of the plurality of high frequency flags are set. In another particular embodiment, the method includes decreasing the clock frequency to a slow mode when none of the plurality of high frequency flags are set.

In still another particular embodiment, the method includes determining whether the at least one of the plurality of master devices is a preferred device prior to setting a high frequency flag. The preferred device can be a processor, an input/output bus controller, a direct memory access (DMA) controller, an error correction code module, and an external memory interface.

In another particular embodiment, the method includes determining a number of master devices requesting bus access, determining whether the number of master devices requesting bus access is greater than a threshold, and setting a high frequency flag for master activity level, when the number is greater than the threshold. In yet another particular embodiment, the method includes clearing a previously set high frequency flag for master activity level, when the number of master devices requesting bus access is less than the threshold.

In another embodiment, a method of controlling a clock frequency of a bus coupled to a plurality of devices is disclosed and includes monitoring a plurality of devices that are coupled to the bus and receiving a bus master request from at least one of the plurality of devices. The bus master request can be a request to communicate via the bus. In this particular embodiment, the method also includes determining whether the at least one of the plurality of devices is a preferred device and setting a high frequency flag for the at least one of the plurality of devices when the at least one of the plurality of devices is a preferred device.

In yet another embodiment, a method of controlling a clock frequency of a bus coupled to a plurality of devices is disclosed and includes monitoring a plurality of devices that are coupled to the bus, determining a number of master devices that are requesting bus access, determining whether the number of master devices that are requesting bus access is greater than a threshold, and setting a high frequency flag for master activity level when the number is greater than the threshold.

In still another embodiment, a system is disclosed and includes a bus, at least one master device that is coupled to the bus, at least one slave device that is coupled to the bus, and a clock controller that is coupled to the at least one master device. The clock controller can output a variable clock frequency that varies in response to one or more inputs from the at least one master device.

In yet still another embodiment, a system is disclosed and includes a bus and a first master device that is coupled to the bus. The first master device can provide a first trigger input as a request to increase a variable clock frequency. Further, the system includes a programmable clock controller that has a computer program embedded therein. In this embodiment, the computer program includes instructions to adjust the variable clock frequency in response to the first trigger input. The variable clock frequency is provided in response to the request.

The functionality of various systems, modules, circuits, devices or components described herein may be implemented as hardware (including discrete components, integrated circuits and systems-on-a-chip 'SoC'), firmware (including application specific integrated circuits and programmable chips) and/or software or a combination thereof, depending on the application requirements.

FIG. **1** depicts an electronic system, generally designated **100**, that includes a plurality of devices connected by a bus **102**, according to an illustrative embodiment. In a particular embodiment, the bus **102** is an advanced microprocessor bus architecture (AMBA) type of bus used for SoC interconnects. In another embodiment, the bus **102** may be based on a proprietary bus communication standard or may be based on other published standards.

An arbiter **110** is coupled to the bus **102**. In addition, at least one master device that includes a first master device **120** and

a second master device **122** and at least one slave device that includes a first slave device **130** and a second slave device **132** are coupled to the bus **102**. Further, a clock controller **150** is coupled to the arbiter **110** and a clock **140** is coupled to the clock controller **150**. In an alternative embodiment, the clock **140** can be integrated with the clock controller **150**.

FIG. **1** also shows a central processing unit (CPU) **104** coupled to the clock controller **150**. As further shown, the first master device **120** and the second master device **122** are each coupled to the clock controller **150** and the arbiter **110**.

In a particular embodiment, the arbiter **110** controls the flow of data on the bus **102** including the bus timing. The first master device **120** may initiate communication with the first slave device **130** by requesting an access token from the arbiter **110** to communicate over the bus **102**. The first slave device **130** may receive data but may not initiate communication with a master. That is, the first slave device **130** is disabled to initiate communication with the plurality of devices coupled to the bus **102**. In an alternative embodiment, more than two master devices and/or more than two slave devices may be coupled to the bus **102**.

In an exemplary embodiment, the first master device **120** can be a processor, an input/output bus controller, a direct memory access (DMA) controller, an error correction code module or an external memory interface. Examples of the slave device **130** may include an on-chip memory, an off-chip memory, a flash controller, a power supply controller, or any other peripheral device or controller.

In an illustrative embodiment, the clock **140** provides a clock signal to the clock controller **150**. The clock signal received by the clock controller **150** can be altered within the clock controller **150**. The clock controller **150** can output a high speed clock **152** having a variable clock frequency to the bus **102** via the arbiter **110** and another high speed clock output to the CPU **104**. Further, the clock controller **150** can output a low speed clock output to a low speed bus **106**. In an exemplary embodiment, the clock controller **150** can output the high speed clock **152** directly to the bus **102**.

In an alternative embodiment, the high speed clock **152** and the low speed output can be provided to additional master or slave devices such as the device **170** based on the application requirements. In an exemplary embodiment, the clock controller **150** outputs a clock frequency that is variable or adjustable. In other words, the clock frequency of the high speed clock **152** is adjustable to meet a desired output of the device while reducing power consumed by the device. Since power consumption is proportional to the number of transitions on the logic, a decrease in the selectable clock frequency (selected during light load conditions) causes a corresponding decrease in power consumed by the devices coupled to the bus **102**, such as the master devices **120**, **122**.

In a particular embodiment, the clock frequency of the high speed clock **152** may be varied between a minimum frequency and a maximum frequency. The specific values for the upper and lower limit of the frequency range may vary and may depend on the application. In a particular embodiment, the maximum clock frequency is 100 megahertz (MHz) and the minimum clock frequency is 1000 kilohertz (kHz). In a particular embodiment, a typical value for the variable clock frequency of the high speed clock **152** may be 100 megahertz. In one embodiment, the clock frequency is selected to be at the maximum frequency divisible by a factor of 1, 2, 4, 8 or 16.

Each of the plurality of devices coupled to the bus **102** provide a corresponding trigger output. Each of the trigger outputs may be triggered or enabled in response to an event such as a desired increase in device performance. For example, an occurrence of an increase (or decrease) in output and/or an increase (or decrease) in needed performance due to loading of the device measured within a predefined time interval may trigger the event output. An example of a load or an output of a device may include a level of audio processing or signal output of an MP3 player. As another example, an occurrence of a change in power consumed by the device may trigger the event output. In a particular embodiment, the predefined time interval may vary from one microsecond to several milliseconds. In another embodiment, the trigger output is generated when the increase (or decrease) in the device output is above a threshold. As yet another example, the arbiter **10** detects change in the flow of data on the bus **102** and generates a trigger event.

The generation of the trigger output is indicative of a request to change the clock frequency of the high speed clock **152**. That is, the device provides the trigger output when a predefined change occurs in the device performance such as a variation in the load or the output of the device.

In a particular embodiment, the plurality of trigger outputs are received by the clock controller **150** as corresponding trigger signal inputs. The clock controller **150** controls and/or adjusts the high speed clock **152** by changing the clock frequency in response to the plurality of trigger signal inputs. That is, the clock frequency of the high speed clock **152** may be adjusted and provided as an output to directly control the clock frequency of other devices such as the second master device **122** and/or provided as an output to the arbiter **110** for controlling speed of the bus **102**.

In an alternative embodiment, the plurality of trigger outputs are received by the arbiter **110** as corresponding trigger signal inputs respectively. The clock controller **150** controls the arbiter **110**. The arbiter **110** communicates with the clock controller **150** to request changes in frequency. The arbiter **110** controls and/or adjusts a clock frequency of the bus **102** in response to receiving the plurality of trigger signal inputs. That is, the arbiter **110** adjusts an input clock to provide the adjusted clock frequency for controlling the speed of the bus **102**. In a particular embodiment, the input clock is the high speed clock **152** and the high speed clock **152** may be further adjusted or passed through to the bus **102**.

In a particular embodiment, the clock controller **150** processes each of the trigger signal inputs and provides the high speed clock **152** based on the particular inputs. That is, the clock controller **150** adjusts the clock frequency differently based on which ones of the trigger signal inputs have been enabled. For example, the trigger signal input from a particular or preferred master device may be viewed to have a higher priority compared to other inputs. As another example, the clock controller **150** may adjust the clock frequency when at least n inputs of the plurality of trigger signal inputs have been enabled. Preferred devices may be selected by comparing device attributes such as power consumption for a predefined clock frequency. In a particular embodiment, the preferred device may include a master device that consumes more power at a predefined frequency compared to another master device that consumes less power at the same frequency.

In a particular embodiment, the clock controller **150** may determine that a change in the high speed clock **152** may not be desired. In this embodiment, adjusting the frequency selection output may include not changing the variable clock frequency in response to the trigger inputs. For example, if the clock frequency is already at the maximum frequency then an increase in the device output may not result in a corresponding increase in the clock frequency. In a particular embodiment, the variable clock frequency is selected to be equal to the minimum clock frequency when all of the plurality of

trigger outputs are disabled. Operation in this mode results in additional power savings compared to operating modes when at least some of the plurality of trigger outputs are enabled.

In a particular embodiment, the clock controller **150** may be implemented as a programmable device having an embedded computer program **156**. The computer program **156** includes one or more instructions to perform various functions such as adjusting the high speed clock **152** in response to one or more of the trigger inputs. The high speed clock **152** is provided to at least one device for changing the clock frequency in response to a trigger input.

In a particular embodiment, the clock controller **150** is programmable to differentiate each of the trigger inputs. That is, the clock controller **150** adjusts the selected clock frequency differently based on which ones of the trigger inputs have been enabled. For example, the trigger input from a particular or preferred master device may be programmed to have a higher priority compared to other inputs. As another example, the clock controller **150** may be programmed to change the selected clock frequency when at least n inputs of the plurality of trigger inputs have been enabled.

As described earlier, in addition to and/or in lieu of controlling the clock frequency by the clock controller **150**, the arbiter **10** may be used to control the speed of the bus **102** by adjusting the clock frequency provided to the bus **102**. In a particular embodiment, the arbiter **110** may include a computer program **158** to control the clock frequency of the clock signal provided to the bus **102**. That is, the computer program **158** includes one or more instructions to selectively slow down and/or speed up certain devices coupled to the bus **102**. For example, the computer program **158** may selectively slow down the second master device **122** to match the throughput performance of a slave memory device being accessed by the second master device **122**.

In a particular embodiment, the computer program **158** may differentiate between master devices and/or slave devices coupled to the bus **102**. That is, the arbiter **110** adjusts the clock frequency of the bus **102** differently based on which ones of the master devices request communication. For example, the token request from a particular master device may be programmed to have a higher priority compared to others. As another example, the arbiter **110** may be programmed to change the clock frequency of the bus **102** when at least n master devices coupled to the bus **102** have requested communication.

FIG. **2** is a flow chart illustrating a method of setting bus speed control flags within an electronic system is shown and commences at block **200**. In a particular embodiment, the electronic system is the system **100** illustrated in FIG. **1**. Commencing at block **200**, a controller, e.g., an arbiter or clock controller, monitors one or more master devices. At block **202**, the controller receives a request to increase bus speed from a master device.

Moving to decision step **204**, the controller determines whether to enable the request to increase the bus speed. If so, the method proceeds to block **206** and the controller sets a high frequency flag for the particular device. Next, at decision step **208**, the controller determines whether the power to the system is turned off. If so, the method ends at state **210**. On the other hand, if the power to the system remains on, the method returns to block **200** and continues as described herein.

Returning to decision step **204**, if the controller determines not to enable the request to increase the bus speed, the method moves to block **212** and the controller clears the high frequency flag for the particular device. The method then proceeds to decision step **208** and continues as described herein.

Referring to FIG. **3**, a flow chart illustrating an alternative method of setting bus speed control flags within an electronic system is shown. Beginning at block **300**, a controller, e.g., an arbiter or a clock controller, monitors one or more master devices. At block **302**, the controller receives a bus master request from a master device. Moving to decision step **304**, the controller determines whether the master device is a preferred device. In a particular embodiment, the arbiter may make this determination by comparing the master device to a predefined list of preferred devices.

At decision step **304**, when the controller determines that the master device that sent the bus master request is a preferred device, the method proceeds to step **306** and the controller sets a high frequency flag for the particular master device. Next, at decision step **308**, the controller determines whether the power to the system is turned off. If so, the method ends at state **310**. On the other hand, if the power to the system remains on, the method returns to block **300** and continues as described herein.

Returning to decision step **304**, if the controller determines that the master device is not a preferred device, the method proceeds to block **312** and the controller clears the high frequency flag for the particular master device. The method then proceeds to decision step **308** and continues as described herein.

FIG. **4** is a flow chart illustrating another alternative embodiment of a method of setting bus speed control flags within an electronic system is shown. Starting at step **400**, a controller, e.g., an arbiter or a clock controller, monitors each one of a plurality of master devices coupled to a bus. Next, at step **402**, the controller receives a bus master request from a master device. Moving to step **404**, the controller determines the number of master devices requesting bus access.

At decision step **406**, the controller determines whether the number of master devices requesting bus access is greater than a threshold. If so, the method proceeds to block **408** and the controller sets a high frequency flag for master activity level. Next, at decision step **410**, the controller determines whether the power to the system is turned off. If so, the method ends at state **412**. On the other hand, if the power to the system remains on, the method returns to block **400** and continues as described herein.

Returning to decision step **406**, if the controller determines that the number of master devices requesting bus access is not greater than the threshold, the method continues to block **414**. At block **414**, the controller clears the high frequency flag for master activity level. The method then proceeds to decision step **410** and continues as described herein.

Referring to FIG. **5**, a flow chart illustrating yet another alternative of a method of setting bus speed control flags within an electronic system is shown. Beginning at block **500**, a controller monitors one or more slave devices. At block **502**, the controller receives a bus master request from a slave device. Moving to decision step **504**, the controller determines whether the slave device is a preferred device. In a particular embodiment, the arbiter may make this determination by comparing the slave device to a predefined list of preferred devices.

At decision step **504**, when the controller determines that the slave device that sent the bus master request is a preferred device, the method proceeds to step **506** and the controller sets a high frequency flag for the particular slave device. Next, at decision step **508**, the controller determines whether the power to the system is turned off. If so, the method ends at state **510**. On the other hand, if the power to the system remains on, the method returns to block **500** and continues as described herein.

Returning to decision step **504**, if the controller determines that the slave device is not a preferred device, the method proceeds to block **512** and the controller clears the high frequency flag for the particular slave device. The method then proceeds to decision step **508** and continues as described herein.

Referring to FIG. **6**, a method of monitoring one or more speed control flags within an electronic system is shown and commences at block **600**. At block **600**, a controller, e.g., an arbiter or clock controller, monitors all speed control flags within the electronic system. Moving to decision step **602**, the controller determines whether any flag is set. If so, the method proceeds to block **604** and the controller increases the clock frequency to a normal mode. Thereafter, the method proceeds to decision step **606** and the controller determines whether the power to the system is turned off. If so, the method ends at state **608**. On the other hand, if the power to the system is not turned off, the method returns to block **600** and continues as described herein.

Returning to decision step **602**, when the controller determines that the speed control flags are not set, the method proceeds to block **610** and the controller decreases the clock frequency to a slow mode. The method then continues to decision step **606** and continues as described herein.

In each of the methods described herein, various steps described above may be added, omitted, combined, altered, or performed in different orders.

For purposes of this disclosure, the disclosed system may include any instrumentality or aggregate of instrumentalities operable to perform functions such as transmit, receive, compute, classify, process, retrieve, originate, switch, store, display, manifest, detect, record, reproduce, handle, or utilize any form of information, intelligence, or data for consumer, business, scientific, control, or other purposes. For example, the system **100** may be implemented as one or more integrated circuits, a printed circuit board, a processor, or any other suitable device and may vary in size, shape, performance, functionality, and price. It should be understood that the term "computer system" or "program" is intended to encompass any device having a logic circuit that executes instructions from a memory medium.

Although illustrative embodiments have been shown and described, a wide range of modification, change and substitution is contemplated in the foregoing disclosure and in some instances, certain features of the embodiments may be employed without a corresponding use of other features. For example, while certain aspects of the present disclosure have been described in the context of the system **100** having one or more devices, those of ordinary skill in the art will appreciate that the processes disclosed are capable of being implemented using discrete components and/or SoC. As an additional example, it is contemplated that additional clocks used within the system may be similarly controlled to gain additional savings in power consumption.

The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the true scope of the present invention. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

What is claimed is:

1. A method comprising:

monitoring a plurality of master devices coupled to a bus;

receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

in response to receiving the request from the first master device:

providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and

providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

2. The method of claim **1**, wherein the first master device performs a clock-frequency evaluation prior to generating the request.

3. The method of claim **2**, wherein the clock-frequency evaluation results in setting a high-speed clock flag.

4. The method of claim **1**, wherein the predefined time interval is from one microsecond to several milliseconds.

5. The method of claim **1**, wherein the loading of the first master device includes a level of audio processing.

6. The method of claim **5**, wherein the audio processing comprises audio processing of a Moving Picture Experts Group Phase 1 (MPEG-1) Audio Layer-3 (MP3) player.

7. The method of claim **1**, wherein controlling the clock frequency of the bus comprises adjusting the clock frequency of the bus.

8. The method of claim **1**, wherein the request to change the clock frequency of the high-speed clock comprises a request to increase the clock frequency of the high-speed clock.

9. The method of claim **1**, wherein the predefined change in performance comprises a variation in output of the first master device.

10. The method of claim **9**, wherein the output of the first master device comprises a signal output.

11. The method of claim **10**, wherein the signal output comprises a signal output of a Moving Picture Experts Group Phase 1 (MPEG-1) Audio Layer-3 (MP3) player.

12. The method of claim **1**, wherein the predefined change in performance comprises a change in power consumed by the first master device.

13. The method of claim **7**, wherein adjusting the clock frequency of the bus comprises adjusting the variable clock frequency of the bus from a non-zero value to another non-zero value without stopping a clock.

14. A system comprising:

a bus capable of operation at a variable clock frequency;

a first master device coupled to the bus, the first master device configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

a programmable clock controller having an embedded computer program therein, the computer program including instructions to:

receive the request provided by the first master device;

provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device; and

provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

15. The system of claim **14**, wherein the computer program further includes instructions to adjust the variable clock frequency of the bus to a predetermined frequency when no request is received from the first master device.

16. The system of claim **14**, wherein the first master device performs a clock-frequency evaluation prior to generating the request, and wherein the loading of the first master device includes a level of audio processing of a Moving Picture Experts Group Phase 1 (MPEG-1) Audio Layer-3 (MP3) player.

17. The system of claim **14**, wherein the instructions to provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus include instructions to adjust the clock frequency of the bus.

18. A system comprising:

a bus capable of operation at a variable clock frequency;

a first master device coupled to the bus;

an arbiter coupled to the bus and coupled to the first master device, the arbiter configured to control flow of data on the bus; and

a clock controller coupled to the arbiter and coupled to the first master device, the clock controller configured to output a clock frequency of a high-speed clock to control the variable clock frequency of the bus and to control a clock frequency of a second master device coupled to the bus, the clock controller configured to receive a request to change the clock frequency of the high-speed clock from the first master device, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the clock controller is configured to adjust the variable clock frequency of the bus in response to receiving the request from the first master device, and wherein the predefined change in the performance is due to loading of the first master device as measured within a predefined time interval.

19. The system of claim **18**, wherein the first master device performs a clock-frequency evaluation prior to generating the request and wherein the change in performance comprises a change in power consumed by the first master device.

20. The system of claim **18**, wherein the clock controller automatically adjusts the variable clock frequency of the bus to a predetermined frequency when no requests are received from the first master device.

21. The system of claim **18**, wherein adjusting the variable clock frequency of the bus comprises decreasing the clock frequency of the bus.

22. The system of claim **18**, wherein adjusting the variable clock frequency of the bus comprises selecting the variable clock frequency to be a frequency divisible by a factor of 1, 2, 4, 8, or 16.

23. The system of claim **18**, wherein the predefined change in the performance of the first master device comprises a variation in a signal output of a Moving Picture Experts Group Phase 1 (MPEG-1) Audio Layer-3 (MP3) player.

24. The system of claim **18**, wherein the predefined change in the performance of the first master device comprises a variation in load of the first master device.

25. The system of claim **24**, wherein the load of the first master device includes a level of audio processing of a Moving Picture Experts Group Phase 1 (MPEG 1) Audio Layer-3 (MP3) player.

26. The system of claim **18**, wherein the predefined change in the performance of the first master device comprises a change in power consumed by the first master device and wherein the request to change the variable clock frequency of the bus comprises a request to increase the variable clock frequency of the bus.

27. The system of claim **18**, wherein adjusting the variable clock frequency of the bus comprises adjusting the variable clock frequency of the bus from a non-zero value to another non-zero value without stopping a clock.

* * * * *

CERTIFICATE OF SERVICE

I hereby certify that, on this 14th day of September, 2022, I filed the foregoing Non-Confidential Brief for Defendant-Appellant Intel Corporation with the Clerk of the United States Court of Appeals for the Federal Circuit via the CM/ECF system, which will send notice of such filing to all registered CM/ECF users.

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September 14, 2022

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September 14, 2022